1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

"Finny"

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

08 JANUARY 2008

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4	4	BOM Configuration	N/A K2_MASTER
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7	7	Functional / ICT Test	N/A K2_MASTER
8	9	GROUNDING ALIASES	N/A K2_MASTER
9	10	CPU FSB	N/A K2_MASTER
10	11	CPU Power & Ground	N/A K2_MASTER
11	12	CPU Decoupling & VID	N/A K2_MASTER
12	13	eXtended Debug Port (XDP)	11/06/2006 T9_MLB_NOME
13	14	NB CPU Interface	10/30/2006 T9_MLB
14	15	NB PEG / Video Interfaces	10/30/2006 T9_MLB
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17	18	NB Power 1	10/30/2006 T9_MLB
18	19	NB Power 2	10/30/2006 T9_MLB
19	20	NB Grounds	10/30/2006 T9_MLB
20	21	NB Standard Decoupling	N/A K2_MASTER
21	22	NB Graphics Decoupling	N/A K2_MASTER
22	23	SB Enet, Disk, FSB, LPC	06/08/2007 T9_MLB_NOME
23	24	SB PCI, PCIe, DMI, USB	06/08/2007 T9_MLB_NOME
24	25	SB Pwr Mgt, GPIO, Clink	06/08/2007 T9_MLB_NOME
25	26	SB Power & Ground	06/08/2007 T9_MLB_NOME
26	27	SB Decoupling	N/A K2_MASTER
27	28	SB Misc	N/A K2_MASTER
28	29	Clock (CK505)	N/A K2_MASTER
29	30	Clock Termination	N/A K2_MASTER
30	31	DDR2 SO-DIMM Connector A	N/A K2_MASTER
31	32	DDR2 SO-DIMM Connector B	N/A K2_MASTER
32	33	Memory Active Termination	N/A K2_MASTER
33	34	PCI-E MiniCard Connector	N/A K2_MASTER
34	37	Ethernet (Yukon)	N/A K2_MASTER
35	38	YUKON/ULTRA SUPPORT	N/A K2_MASTER
36	39	ETHERNET CONNECTOR	N/A K2_MASTER
37	40	FW: 1394B CONTROLLER	N/A K2_MASTER
38	42	FW: 1394B MISC	N/A K2_MASTER
39	43	FIREWIRE CONNECTORS	N/A K2_MASTER
40	44	PATA Connector	N/A K2_MASTER
41	45	SATA Connectors	N/A K2_MASTER
42	46	EXTERNAL USB CONNECTORS	N/A K2_MASTER
43	47	Internal USB Connections	N/A K2_MASTER
44	49	SMC	12/15/2006 T9_MLB_NOME
45	50	SMC Support	N/A K2_MASTER
46	51	LPC+ Debug Connector	06/08/2007 T9_MLB_NOME
47	52	SMBUS CONNECTIONS	N/A K2_MASTER
48	53	Current & Voltage Sensing	N/A K2_MASTER
49	55	Thermal Sensors	N/A K2_MASTER
50	56	HD AND OD FAN	N/A K2_MASTER
51	57	CPU FAN	N/A K2_MASTER
52	61	SPI BootROM	06/08/2007 T9_MLB_NOME
53	69	POWER SEQUENCING BLOCK DIAGRAM	N/A K2_MASTER
54	70	PGOOD and Power Sequencing	N/A K2_MASTER
55	71	IMVP6 CPU VCore Regulator	N/A K2_MASTER
56	72	IMVP6 3RD PHASE	N/A K2_MASTER
57	73	1.5V / 1.05V SUPPLIES	N/A K2_MASTER
58	74	1.25V / MCH CORE SUPPLIES	N/A K2_MASTER
59	75	1.8V S3 /0.9V S0 SUPPLIES	N/A K2_MASTER
60	76	5V S5 / 3.3V S3 SUPPLIES	N/A K2_MASTER
61	77	3.3V / 2.5V POWER SUPPLIES	N/A K2_MASTER
62	78	S3 & S0 FETs	N/A K2_MASTER
63	84	MXM PCI-E & PWR	N/A K2_MASTER
64	85	MXM I/O	N/A K2_MASTER
65	90	INTERNAL DISPLAY CONNS	N/A K2_MASTER
66	91	Analog Video Support	N/A K2_MASTER
67	94	External Display Conns	N/A K2_MASTER
68	98	MLB: AUDIO CONNECTOR	N/A K2_MASTER
69	100	CPU/FSB Constraints	09/27/2006 T9_MLB
70	101	NB Constraints	09/27/2006 T9_MLB
71	102	Memory Constraints	09/27/2006 T9_MLB
72	103	SB Constraints (1 of 2)	09/27/2006 T9_MLB
73	104	SB Constraints (2 of 2)	(10/02/2006) (MASTER)
74	105	Clock Constraints	09/27/2006 T9_MLB
75	106	FireWire & SMC Constraints	09/27/2006 T9_MLB
76	108	M72/M78 SPECIFIC CONSTRAINTS	09/27/2006 T9_MLB
77	109	M72/M78 RULE DEFINITIONS	09/27/2006 T9_MLB
78	110	Cross Reference Page	
79	111	Cross Reference Page	
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82	114	Cross Reference Page	
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86	118	Cross Reference Page	

DRAWING
TITLE=M72
ABBREV=DRAWING
LAST_MODIFIED=Tue Jan 8 14:37:55 2008

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

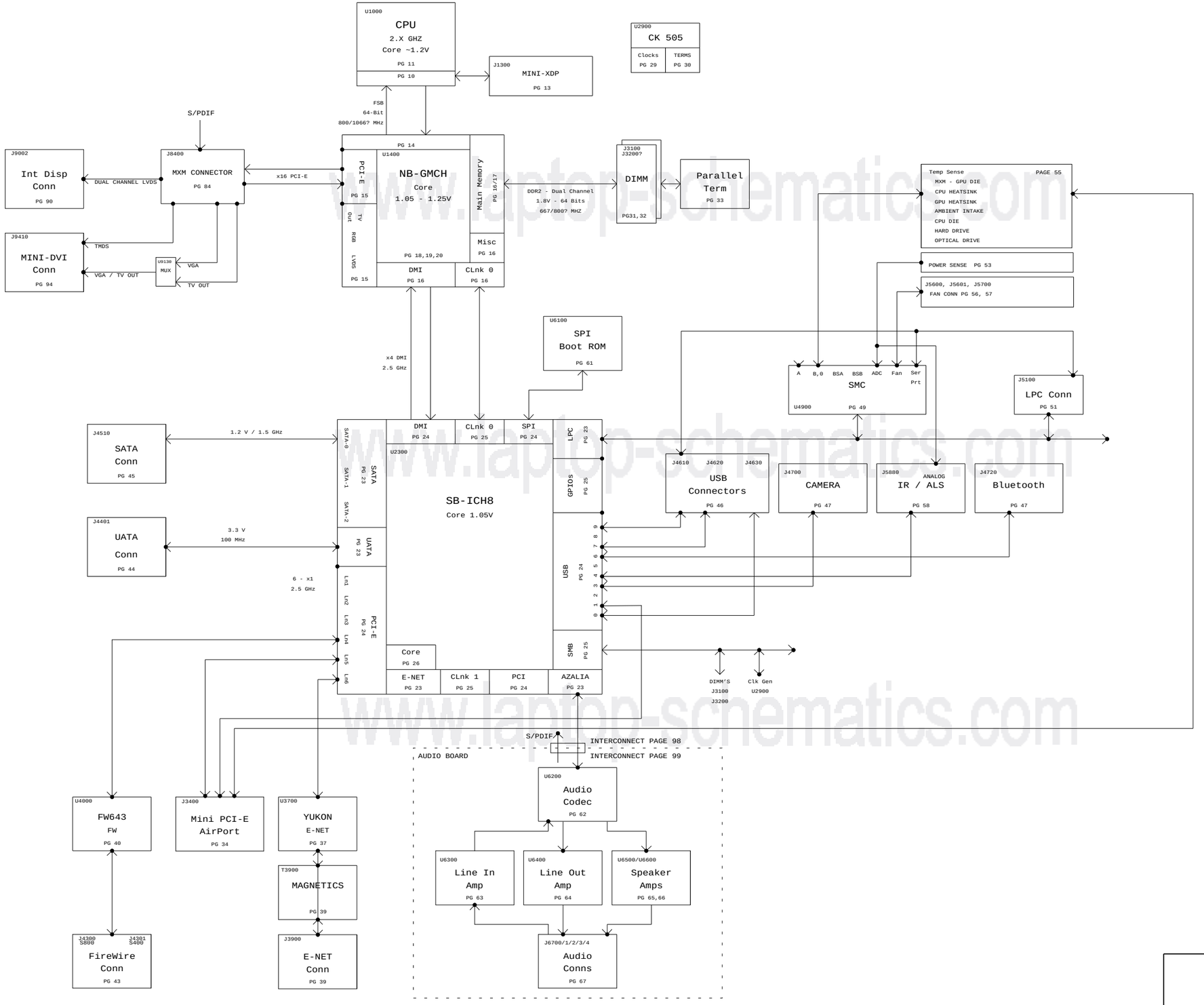
SIZE D

APPLE INC.

TITLE
SCH,"Finny",MLB

DRAWING NUMBER 051-7388 REV. A

SHT 1 OF 118

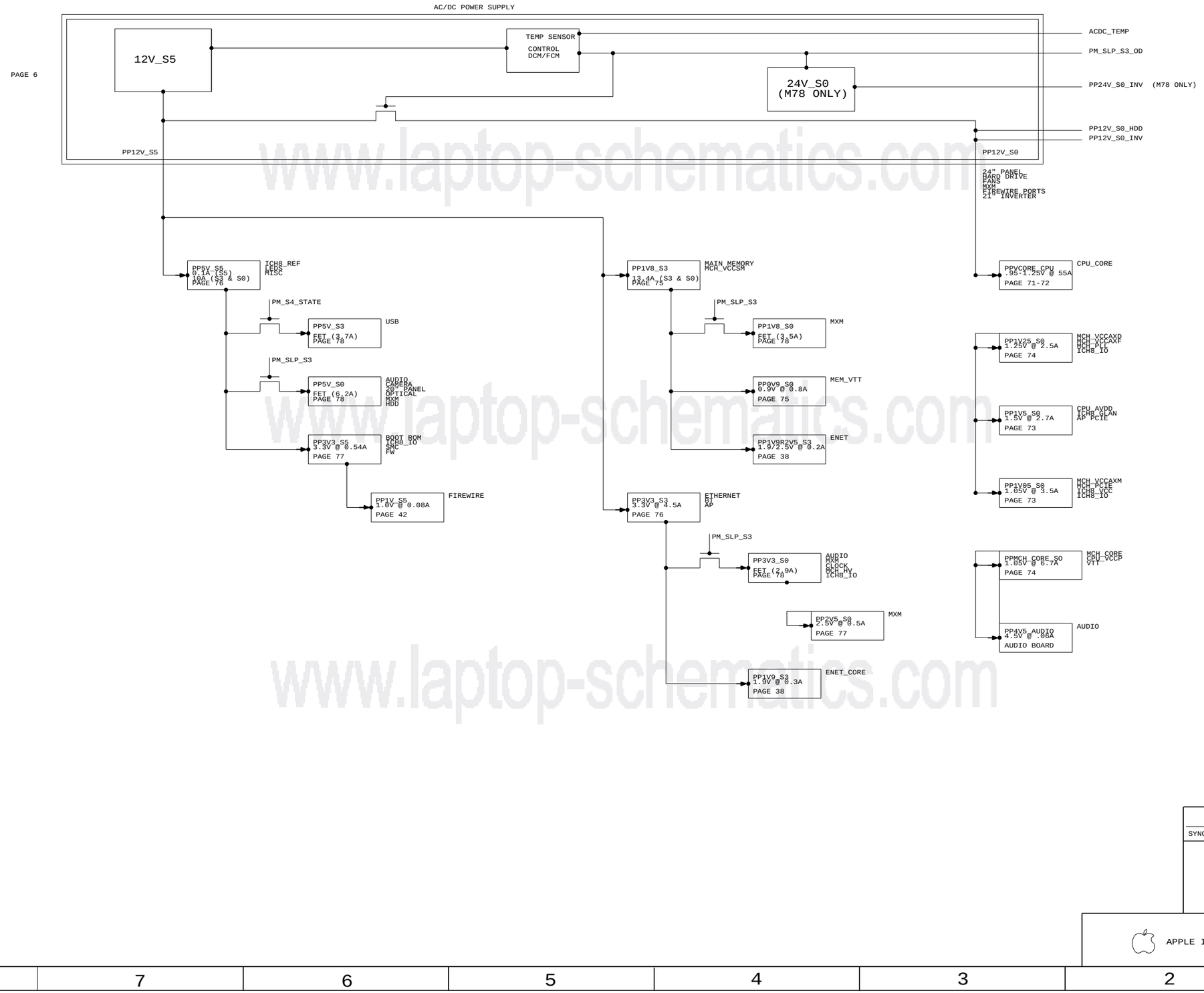


System Block Diagram

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 2 OF 118	



Power Block Diagram

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 3 OF 118	

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
630-9183	PCBA,K3,MLB,BEST	24_INCH_LCD,2P8GHZ_CPU,BASIC,CR_STD,12V_PWR_SENSE
630-9215	PCBA,K3,MLB,CTO	24_INCH_LCD,3P06GHZ_CPU,BASIC,CR_STD,12V_PWR_SENSE
607-2079	K3 MLB DEVELOPMENT	DEVELOPMENT,XDP_CONN,LPCPLUS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-8956	PCBA,MLB,K2,GOOD	20_INCH_LCD,2P4GHZ_CPU,BASIC,CR_STD,K2_GOOD
630-9214	PCBA,MLB,K2,BETTER	20_INCH_LCD,2P66GHZ_CPU,BASIC,CR_STD,12V_PWR_SENSE,K2_BETTER
607-1336	K2 MLB DEVELOPMENT	DEVELOPMENT,XDP_CONN,LPCPLUS

BOM GROUPS

BOM GROUP	BOM OPTIONS
BASIC	5V1V8REG_SKIP,ALTERNATE,COMMON,XDP,MXM_ROM,NBCFG_PEG_REVERSE,TMDS_RES_0_OHM,MXM_PWR_SENSE,2V5_S0_REG,CPU_TDIODE,PRODUCTION

CPUS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S3582	1	IC,PDC,PRQ,C0,3.06G,1066FSB,6M,55W,PGA	CPU	CRITICAL	3P06GHZ_CPU
337S3581	1	IC,PC,PRQ,C0,2.8G,1066FSB,6M,55W,PGA	CPU	CRITICAL	2P8GHZ_CPU
337S3580	1	IC,PDC,PRQ,C0,2.66G,1066FSB,6M,55W,PGA	CPU	CRITICAL	2P66GHZ_CPU
337S3579	1	IC,PDC,PRQ,C0,2.4G,1066FSB,6M,55W,PGA	CPU	CRITICAL	2P4GHZ_CPU

MISC.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0306	4	FLTR,CMN MDE,90 OHM,200MA,LF2012	L9400,L9401,L9402,L9403	CRITICAL	TMDS_CHOKE
116S0004	8	RES,0-OHM,1/16W,5%,0402	R9400,R9402,R9403,R9404,R9405,R9408,R9409,R9415		TMDS_RES_0_OHM

COMMON

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	338S0569	1	IC,NB,CRESTLINE,XM,C0,PRQ	U1400	CRITICAL	
	338S0434	1	IC,SB,ICH8M,B1,PRQ	U2300	CRITICAL	
	338S0523	1	IC,FW643-06,1394B	U4000	CRITICAL	
537 - 359S0127	359S0130	1	CK505 - SILEGO SLG2AP101	U2900	CRITICAL	
	820-2149	1	PCB,FAB,IO ALIGNMENT,M72	IO1	CRITICAL	
	825-6447	1	MLB LABEL,48.0X4.8	X14	CRITICAL	
	341T0112	1	EFI ROM,K2/K3	U6100	CRITICAL	

PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
	051-7388	1	PCB,SCHEM,MLB,K2	SCH1		20_INCH_LCD
056-2483 (MCO) 057-0497 (PANEL)	820-2223	1	PCB,FAB,MLB,K2,HF	MLB1		20_INCH_LCD
(338S0274 - BLNK)	341T0113	1	IC,SMC,K2	U4900	CRITICAL	20_INCH_LCD
	114S0312	1	RES,9.31K,0402,1%,1/16W,LF	R7117		20_INCH_LCD
	132S0205	1	CAP,CER,270PF,10%,50V,0402	C7113		20_INCH_LCD
	132S0178	1	CAP,CER,0.47UF,10%,6.3V,0402	C7128		20_INCH_LCD
	132S0082	1	CAP,CER,0.068UF,10%,10V,0402	C7134		20_INCH_LCD
MXM ROM (335S0155 - BLNK) (341S2233 - K2)	335S0155	1	IC,2K I2C EEPROM,BLANK	U8570	CRITICAL	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602			CAP
124-0369	124-0363		C7109,C7154,C7254,C7340,C7440,C7480,C7530,C7532	CAP
124-0371	124-0363		C7109,C7154,C7254,C7340,C7440,C7480,C7530,C7532	CAP
124-0361	124-0370		C7490,C7491	CAP
126S0118	126S0086		C1235,C2100,C2120,C2130,C2140	CAP
126S0119	126S0092		C625	CAP
128S0197	128S0114		C1251,C1252,C1253,C1254,C1255	CAP
152S0759	152S0317		L2173	INDUCTOR
152S0758	152S0488		L2703	INDUCTOR
371S0464	371S0154		D7624,D7664	DIODES
359S0142	359S0130		U2900	CLOCK CHIP
155S0232	155S0289		FL4300,FL4310,L4612,L4622,L4632	CHOKE

BOM Configuration

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE NONE SHT 4 OF 118

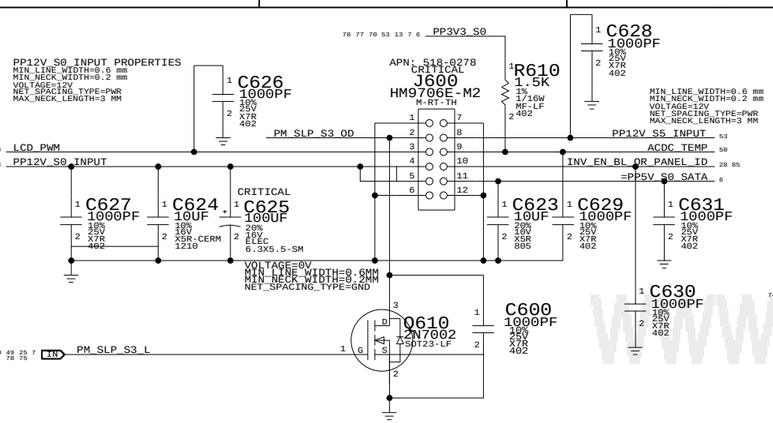
NOTE: All page numbers are .csa, not PDF. See page 1 for .csa -> PDF mapping.

Revision History

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 5 OF 118	



EMC: C600,C626,C627,C628,C629,C630,C631
PLACE AT J600.

"S0" RAILS

ONLY ON IN RUN

- PP0V9_S0 =PP0V9_S0M_MEM_TERM 33
  - MAKE_BASE=TRUE; VOLTAGE=0.9V; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
- PPVCORE_CPU =PPVCORE_S0_CPU 11 12 53
  - MAKE_BASE=TRUE; VOLTAGE=1.25V; MIN_LINE_WIDTH=0.6MM; MIN_NECK_WIDTH=0.3MM; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
- PP1V8_S0 =PP1V8_S0_MXM 84
  - MAKE_BASE=TRUE; VOLTAGE=1.8V; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
- PP2V5_S0 =PP2V5_S0_MXM 85
  - MAKE_BASE=TRUE; VOLTAGE=2.5V; MIN_LINE_WIDTH=0.4 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
- PPMCH_CORE_S0 =PPVCORE_S0_NB 18 21
  - MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PPVCORE_S0_NB_FOLLOW 21
  - =PP1V05_S0_CPU 10 11 12 13 50
  - =PP1V25R1V05_S0_FSB_NB 14 30
  - =PP1V25R1V05_S0_NB_VTT 19 21
  - =PP1V05_S0_SB_CPU_IO 23 26 27
- PP1V05_S0 =PP1V05_S0M_NB_VCCAXM 18 21
  - MAKE_BASE=TRUE; VOLTAGE=1.05V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP1V05_S0_NB_PCIE 21
  - =PP1V05_S0_NB_FOLLOW 21
  - =PPVCORE_S0_SB 26 27
- PP1V5_S0 =PP1V5_S0_CPU 11 12
  - MAKE_BASE=TRUE; VOLTAGE=1.5V; MIN_LINE_WIDTH=0.5 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP1V5_S0_NB_TVDAC 22
  - =PP1V5_S0_SB_VCC1_5_A_ARX 26 27
  - =PP1V5_S0_SB_VCC1_5_A_ATX 26 27
  - =PP1V5_S0_SB_VCCUSBPLL 26 27
  - =PP1V5_S0_SB_VCC1_5_A_USB_CORE 26 27
  - =PP1V5_S0_SB_VCC1_5_A 26
  - =PP1V5_S0_SB 27
  - =PP1V5_S0_MINI 34
- PP1V25_S0 =PP1V25_S0_NB_VCCDMI 19 21
  - MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; VOLTAGE=1.25V; MAKE_BASE=TRUE; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP1V25_S0M_NB_VCCA 21
  - =PP1V25_S0M_NB_VCC 21
  - =PP1V25_S0_NB_PLL 21
  - =PP1V25_S0_NB_VCC 21
  - =PP1V25_S0M_NB_PLL 21
  - =PP1V25_S0_SB_DMI 26 27
- PP3V3_S0 =PP3V3_S0_NB_VCCHV 16 19 21
  - MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP3V3_S0_SB 27
  - =PP3V3_S0_SB_GPIO 23 25
  - =PP3V3_S0_SB_VCCGLAN3_3 26
  - =PP3V3_S0_SB_VCC3_3_PCI 26 27
  - =PP3V3_S0_SB_VCC3_3_IDE 26 27
  - =PP3V3_S0_SB_PCI 24
  - =PP3V3_S0_PM 28
  - =PP3V3_S0_PATA 44
  - =PP3V3_S0_FAN 56 57
  - =PPSPD_S0_MEM 31 32
  - =PP3V3_S0_IMVP 71
  - =PP3V3_S0_AUDIO 98
  - =PP3V3_S0_LPCPLUS 51
  - =PP3V3_S0_SMBUS_SB 52
  - =PP3V3_S0_SMC_LS 50
  - =PP3V3_S0_SMBUS_SMC_0_S0 52
  - =PP3V3_S0_SMBUS_SMC_B_S0 52
  - =PP3V3_S0_SMBUS_SMC_MGMT 52
  - =PP3V3_S0_CK505 29 30
  - =PP3V3_S0_MXM 85
  - =PP3V3_S0_SATALED 45
  - =PP3V3_S0M_CK505 29 30
  - =PP3V3_S0MWOL_SB_CLINK0 25
  - =PP3V3_S0_SB_VCC3_3_DMI 26 27
  - =PP3V3_S0_SB_VCC3_3_SATA 26 27
  - =PP3V3_S0_SB_VCC3_3_VCCPCORE 26
  - =PP3V3R1V5_S0_SB_VCCHDA 26 27
  - =PP3V3_S0MWOL_SB_VCCLAN3_3 26 27
  - =PP3V3_S0MWOL_SB_VCCCL3_3 26 27
  - =PP3V3_S0_TSENS 55
  - =PP3V3_S0_SMC 53
  - =PP3V3_S0_NB_VCCA_PEG_BG 19 21
  - =PP3V3_S0_NB_FOLLOW 21
  - =PP3V3_S0_VIDEO 90 91 94
  - =PP3V3_S0_ENET 38
- PP5V_S0 =PP5V_S0_SB 27
  - MAKE_BASE=TRUE; VOLTAGE=5V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP5V_S0_PATA 44
  - =PP5V_S0_LPCPLUS 7 51
  - =PP5V_S0_AUDIO 98
  - =PP5V_S0_SATA 6
  - =PP5V_S0_MXM 84
  - =PPV_S0_LCD_20INCH 90
- PP12V_S0 =PP12V_S0_FAN 56 57
  - MAKE_BASE=TRUE; VOLTAGE=12V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP12V_S0_AUDIO_SPKRAMP 98
  - =PP12V_S0_CPU 53 71 72
  - =PPV_S0_LCD_24INCH 90
  - =PPV_S0_MXM_PWRSRC 53

"S3" RAILS

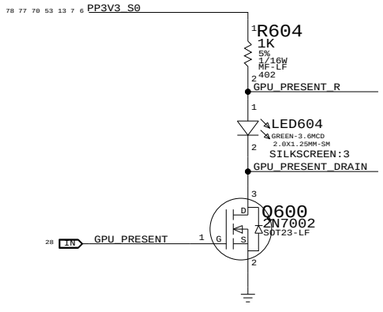
ON IN RUN AND SLEEP

- PP1V8_S3 =PP1V8_S3M_MEM_NB 16 18 21 22
  - MAKE_BASE=TRUE; VOLTAGE=1.8V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP1V8_S3M_NB_VCC 21
  - =PP1V8_S3_MEM 31 32
  - =PP1V8_S3_MEMVTT 75
  - =PP1V8_S3_ENET 38
- PP3V3_S3 =PP3V3_S3_MINI 34
  - MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP3V3_S3_ENET 38 39
  - =PP3V3_S3_BT 47
- PP5V_S3 =PP5V_S3_BNDI 47
  - MAKE_BASE=TRUE; VOLTAGE=5V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP5V_S3_MEMVTT 75

"S5" RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

- PP3V3_S5 =PP3V3_S5_SB 25 27 28
  - MAKE_BASE=TRUE; VOLTAGE=3.3V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP3V3_S5_SB_USB 24
  - =PP3V3_S5_SB_PM 28
  - =PP3V3_S5_SB_VCCSUS3_3 26 27
  - =PP3V3_S5_SB_VCCSUS3_3_USB 26 27
  - =PP3V3_S5_SMBUS_SB_ME 52
  - =PP3V3_S5_FW 40 42 43
  - =PP3V3_S5_SMC 49 50
  - =PP3V3_S5_ROM 61
  - =PP3V3_S5_SB_GPIO 25
  - =PP3V3_S5_SB_CLINK1 25
  - =PP3V3_S5_SB_3V3_VCCSUSHDA 26 27
  - =PP3V3_S5_LPCPLUS 7 51
  - =PP3V3_S5_SMBUS_SMC_BSA 52
  - =PP3V3_S5_FAN 56 57
  - =PP3V3_S5_SMCUSBMUX 46
  - =PP3V3_S5_SMBUS_SMC_A_S5 52
- PP5V_S5 =PP5V_S5_SB 27
  - MAKE_BASE=TRUE; VOLTAGE=5V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PPVIN_S5_SMCVREF 50
  - =PP5V_S5_USB 46
- PP12V_S5 =PP12V_S5_FET
  - MAKE_BASE=TRUE; VOLTAGE=12V; MIN_LINE_WIDTH=0.6 mm; MIN_NECK_WIDTH=0.2 mm; NET_SPACING_TYPE=PWR; MAX_NECK_LENGTH=3 MM
  - =PP12V_S5_FW 43



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0082	1	RES,MF,1/10W,910OHM,5,0603,SMD,LF	R605		20_INCH_LCD
113S0095	1	RES,MF,1/10W,3.3KOHM,5,0603,SMD,LF	R605		24_INCH_LCD

Power Conn / Alias

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 6 OF 118	

FUNCTIONAL TESTPOINTS FOR MAC-1 & ICT

LAYOUT NOTE: PLACE NEAR J1000

100 14 10 7	FSB_A_L<6>	PP1000	PP	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1001	PP	OMIT P4MM
100 14 10 7	FSB_A_L<27>	PP1002	PP	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1003	PP	OMIT P4MM
100 14 10 7	FSB_D_L<0>	PP1004	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1005	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1006	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<0>	PP1007	PP	OMIT P4MM
100 14 10 7	FSB_D_L<16>	PP1008	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1009	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1010	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<1>	PP1011	PP	OMIT P4MM
100 14 10 7	FSB_D_L<41>	PP1012	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1013	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1014	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<2>	PP1015	PP	OMIT P4MM
100 14 10 7	FSB_D_L<59>	PP1016	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1017	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1018	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<3>	PP1019	PP	OMIT P4MM
100 14 10 7	FSB_LOCK_L	PP1020	PP	OMIT P4MM
100 14 13 10	FSB_CPURST_L	PP1021	PP	OMIT P4MM
100 51 23 10	CPU_INIT_L	PP1022	PP	OMIT P4MM
100 23 10	CPU_A20M_L	PP1023	PP	OMIT P4MM
100 23 10	CPU_IGNNE_L	PP1024	PP	OMIT P4MM
100 23 10	CPU_STPCLK_L	PP1025	PP	OMIT P4MM
100 23 10	CPU_INTR	PP1026	PP	OMIT P4MM
100 23 10	CPU_NMI	PP1027	PP	OMIT P4MM
100 23 10	CPU_SMI_L	PP1028	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<0>	PP1029	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<1>	PP1030	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<2>	PP1031	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<3>	PP1032	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<4>	PP1033	PP	OMIT P4MM
105 30 10	FSB_CLK_CPU_P	PP1034	PP	OMIT P4MM
105 30 10	FSB_CLK_CPU_N	PP1035	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U2100

105 30 23	SB_CLK100M_SATA_P	PP2100	PP	OMIT P4MM
105 30 23	SB_CLK100M_SATA_N	PP2101	PP	OMIT P4MM
103 44 23	IDE_PDIOR_L	PP2102	PP	OMIT P4MM
103 44 23	IDE_PDIORDY	PP2103	PP	OMIT P4MM
103 44 23	IDE_PDD<9>	PP2104	PP	OMIT P4MM
104 34 24	PCIE_MINI_D2R_P	PP2105	PP	OMIT P4MM
104 34 24	PCIE_MINI_D2R_N	PP2106	PP	OMIT P4MM
104 37 24	PCIE_ENET_D2R_P	PP2107	PP	OMIT P4MM
104 37 24	PCIE_ENET_D2R_N	PP2108	PP	OMIT P4MM
104 42 40	PCIE_FW_D2R_P	PP2132	PP	OMIT P4MM
104 42 40	PCIE_FW_D2R_N	PP2133	PP	OMIT P4MM
101 24 16	DMI_N2S_P<0>	PP2109	PP	OMIT P4MM
101 24 16	DMI_N2S_N<0>	PP2110	PP	OMIT P4MM
105 30 24 7	SB_CLK100M_DMI_P	PP2111	PP	OMIT P4MM
105 30 24 7	SB_CLK100M_DMI_N	PP2112	PP	OMIT P4MM
49 28 25	PM_SYSRST_L	PP2113	PP	OMIT P4MM
51 49 25 7	PM_CLKRUN_L	PP2114	PP	OMIT P4MM
105 30 25	SB_CLK14P3M_TIMER	PP2115	PP	OMIT P4MM
105 30 25	SB_CLK48M_USBCTLR	PP2116	PP	OMIT P4MM
105 30 24	PCI_CLK33M_SB	PP2117	PP	OMIT P4MM
28 23 7	SB_RTC_RST_L	PP2118	PP	OMIT P4MM
103 45 23	SATA_A_D2R_P	PP2119	PP	OMIT P4MM
103 45 23	SATA_A_D2R_N	PP2120	PP	OMIT P4MM
51 49 23 7	LPC_AD<1>	PP2121	PP	OMIT P4MM
103 47 24	USB_CAMERA_P	PP2122	PP	OMIT P4MM
103 47 24	USB_CAMERA_N	PP2123	PP	OMIT P4MM
103 47 24	USB_IR_P	PP2124	PP	OMIT P4MM
103 47 24	USB_IR_N	PP2125	PP	OMIT P4MM
103 47 24	USB_BT_P	PP2126	PP	OMIT P4MM
103 47 24	USB_BT_N	PP2127	PP	OMIT P4MM
103 61 24	SPI_SCLK_R	PP2128	PP	OMIT P4MM
103 61 24	SPI_SO	PP2129	PP	OMIT P4MM
104 25 16 7	CLINK_NB_CLK	PP2130	PP	OMIT P4MM
104 25 16 7	CLINK_NB_DATA	PP2131	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U1400

100 14 10 7	FSB_A_L<6>	PP1400	PP	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<0>	PP1401	PP	OMIT P4MM
100 14 10 7	FSB_A_L<27>	PP1402	PP	OMIT P4MM
100 14 10 7	FSB_ADSTB_L<1>	PP1403	PP	OMIT P4MM
100 14 10 7	FSB_D_L<0>	PP1404	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<0>	PP1405	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<0>	PP1406	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<0>	PP1407	PP	OMIT P4MM
100 14 10 7	FSB_D_L<16>	PP1408	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<1>	PP1409	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<1>	PP1410	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<1>	PP1411	PP	OMIT P4MM
100 14 10 7	FSB_D_L<41>	PP1412	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<2>	PP1413	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<2>	PP1414	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<2>	PP1415	PP	OMIT P4MM
100 14 10 7	FSB_D_L<59>	PP1416	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_N<3>	PP1417	PP	OMIT P4MM
100 14 10 7	FSB_DSTB_L_P<3>	PP1418	PP	OMIT P4MM
100 14 10 7	FSB_DINV_L<3>	PP1419	PP	OMIT P4MM
100 14 10 7	FSB_LOCK_L	PP1420	PP	OMIT P4MM
100 14 10	FSB_HIT_L	PP1421	PP	OMIT P4MM
100 14 10	FSB_HITM_L	PP1422	PP	OMIT P4MM
100 14 10	FSB_BNR_L	PP1423	PP	OMIT P4MM
100 14 10	FSB_BREQ0_L	PP1424	PP	OMIT P4MM
100 14 10	FSB_DBSY_L	PP1425	PP	OMIT P4MM
100 14 10	FSB_DPWR_L	PP1426	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<0>	PP1427	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<1>	PP1428	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<2>	PP1429	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<3>	PP1430	PP	OMIT P4MM
100 14 10 7	FSB_REQ_L<4>	PP1431	PP	OMIT P4MM
105 30 14	FSB_CLK_NB_P	PP1432	PP	OMIT P4MM
105 30 14 7	FSB_CLK_NB_N	PP1433	PP	OMIT P4MM
71 70 22 16 7	VR_PWRGOOD_DELAY	PP1434	PP	OMIT P4MM
28 16	NB_RESET_L	PP1435	PP	OMIT P4MM
105 30 16	NB_CLK100M_PCIE_P	PP1436	PP	OMIT P4MM
105 30 16 7	NB_CLK100M_PCIE_N	PP1437	PP	OMIT P4MM
101 24 16	DMI_S2N_N<0>	PP1438	PP	OMIT P4MM
101 24 16	DMI_S2N_P<0>	PP1439	PP	OMIT P4MM
22 16	=PP0V9_S3M_MEM_NBVREFA	PP1440	PP	OMIT P4MM
22 16	=PP0V9_S3M_MEM_NBVREFB	PP1441	PP	OMIT P4MM
102 31 17	MEM_A_DQ<7>	PP1442	PP	OMIT P4MM
102 31 17	MEM_A_DQ<14>	PP1443	PP	OMIT P4MM
102 31 17	MEM_A_DQ<16>	PP1444	PP	OMIT P4MM
102 31 17	MEM_A_DQ<25>	PP1445	PP	OMIT P4MM
102 31 17	MEM_A_DQ<39>	PP1446	PP	OMIT P4MM
102 31 17	MEM_A_DQ<47>	PP1447	PP	OMIT P4MM
102 31 17	MEM_A_DQ<54>	PP1448	PP	OMIT P4MM
102 31 17	MEM_A_DQ<59>	PP1449	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<0>	PP1450	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<0>	PP1451	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<1>	PP1452	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<1>	PP1453	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<2>	PP1454	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<2>	PP1455	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<3>	PP1456	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<3>	PP1457	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<4>	PP1458	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<4>	PP1459	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<5>	PP1460	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<5>	PP1461	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<6>	PP1462	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<6>	PP1463	PP	OMIT P4MM
102 31 17	MEM_A_DQS_P<7>	PP1464	PP	OMIT P4MM
102 31 17	MEM_A_DQS_N<7>	PP1465	PP	OMIT P4MM
102 32 17	MEM_B_DQ<6>	PP1466	PP	OMIT P4MM
102 32 17	MEM_B_DQ<8>	PP1467	PP	OMIT P4MM
102 32 17	MEM_B_DQ<23>	PP1468	PP	OMIT P4MM
102 32 17	MEM_B_DQ<25>	PP1469	PP	OMIT P4MM
102 32 17	MEM_B_DQ<38>	PP1470	PP	OMIT P4MM
102 32 17	MEM_B_DQ<44>	PP1471	PP	OMIT P4MM
102 32 17	MEM_B_DQ<48>	PP1472	PP	OMIT P4MM
102 32 17	MEM_B_DQ<62>	PP1473	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<0>	PP1474	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<0>	PP1475	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<1>	PP1476	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<1>	PP1477	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<2>	PP1478	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<2>	PP1479	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<3>	PP1480	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<3>	PP1481	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<4>	PP1482	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<4>	PP1483	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<5>	PP1484	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<5>	PP1485	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<6>	PP1486	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<6>	PP1487	PP	OMIT P4MM
102 32 17	MEM_B_DQS_P<7>	PP1488	PP	OMIT P4MM
102 32 17	MEM_B_DQS_N<7>	PP1489	PP	OMIT P4MM
101 84 15	PEG_D2R_P<7>	PP1490	PP	OMIT P4MM
101 84 15	PEG_D2R_N<7>	PP1491	PP	OMIT P4MM
104 25 16 7	CLINK_NB_CLK	PP1492	PP	OMIT P4MM
104 25 16 7	CLINK_NB_DATA	PP1493	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U3700

105 37 30	PCIE_CLK100M_ENET_P	PP3700	PP	OMIT P4MM
105 37 30	PCIE_CLK100M_ENET_N	PP3701	PP	OMIT P4MM
108 37	PCIE_ENET_R2D_P	PP3702	PP	OMIT P4MM
108 37	PCIE_ENET_R2D_N	PP3703	PP	OMIT P4MM
37 28	ENET_RESET_L	PP3704	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4000

105 40 30	PCIE_CLK100M_FW_P	PP4000	PP	OMIT P4MM
105 40 30	PCIE_CLK100M_FW_N	PP4001	PP	OMIT P4MM
108 40	PCIE_FW_R2D_P	PP4002	PP	OMIT P4MM
108 40	PCIE_FW_R2D_N	PP4003	PP	OMIT P4MM
40 28 7	FW_RESET_L	PP4004	PP	OMIT P4MM

LAYOUT NOTE: PLACE NEAR U4900

105 49 30	PCI_CLK33M_SMC	PP4900	PP	OMIT P4MM
49 28	SMC_LRESET_L	PP4901	PP	OMIT P4MM
51 50 49 7	SMC_RESET_L	PP4902	PP	OMIT P4MM
51 49 23 7	LPC_AD<1>	PP4903	PP	OMIT P4MM

LPC CONNECTOR

51 6	=PP3V3_S5_LPCPLUS	IN	FUNC_TEST=TRUE
51 6	=PP5V_S0_LPCPLUS	IN	FUNC_TEST=TRUE
51	FWH_INIT_L	IN	FUNC_TEST=TRUE
105 51 30	PCI_CLK33M_LPCPLUS	IN	FUNC_TEST=TRUE
51 49 23	LPC_AD<0>	IN	FUNC_TEST=TRUE
51 49 23 7	LPC_AD<1>	IN	FUNC_TEST=TRUE
51 49 23	LPC_AD<2>	IN	FUNC_TEST=TRUE
51 49 23	LPC_AD<3>	IN	FUNC_TEST=TRUE
51 49 23	LPC_FRAME_L	IN	FUNC_TEST=TRUE
51 49 25 7	PM_CLKRUN_L	IN	FUNC_TEST=TRUE
51 24	BOOT_LPC_SPI_L	IN	FUNC_TEST=TRUE
51 50 49	SMC_TMS	IN	FUNC_TEST=TRUE
51 28	DEBUG_RESET_L	IN	FUNC_TEST=TRUE
51 49	SMC_TRST_L	IN	FUNC_TEST=TRUE
51 50 49	SMC_TDO	IN	FUNC_TEST=TRUE
51 49	SMC_MD1	IN	FUNC_TEST=TRUE
51 50 49 46	SMC_TX_L	IN	FUNC_TEST=TRUE
51 49 25	INT_SERIRQ	IN	FUNC_TEST=TRUE
51 50 49 25 7	PM_SUS_STAT_L	IN	FUNC_TEST=TRUE
51 50 49	SMC_TDI	IN	FUNC_TEST=TRUE
51 50 49	SMC_TCK	IN	FUNC_TEST=TRUE
51 50 49 7	SMC_RESET_L	IN	FUNC_TEST=TRUE
51 49	SMC_NMI	IN	FUNC_TEST=TRUE
51 50 49 46	SMC_RX_L	IN	FUNC_TEST=TRUE
51 25	LINDACARD_GPIO	IN	FUNC_TEST=TRUE

16 TP'S

PWROK SEQUENCING

84 70 50 49 7	ALL_SYS_PWRGD	IN	FUNC_TEST=TRUE
70 28 25 7	PM_SB_PWROK	IN	FUNC_TEST=TRUE

STARTUP (BOOT/WAKE) TIMING

71 49	IMVP_VR_ON	IN	FUNC_TEST=TRUE
28 25	VR_PWRGD_CLKEN	IN	FUNC_TEST=TRUE
71 70 22 16 7	VR_PWRGOOD_DELAY	IN	FUNC_TEST=TRUE
70 28 25 7	PM_SB_PWROK	IN	FUNC_TEST=TRUE

SHUTDOWN/SLEEP TIMING

51 50 49 25 7	PM_SUS_STAT_L	IN	FUNC_TEST=TRUE
78 75 70 49 25 6	PM_SLP_S3_L	IN	FUNC_TEST=TRUE
78 75 49 46 25 7	PM_S4_STATE_L	IN	FUNC_TEST=TRUE
84 70 50 49 7	ALL_SYS_PWRGD	IN	FUNC_TEST=TRUE
100 23 13 10	CPU_PWRGD	IN	FUNC_TEST=TRUE

"S0" RAILS

75 70 6	PP0V9_S0	IN	FUNC_TEST=TRUE
72 71 6	PPVCORE_CPU	IN	FUNC_TEST=TRUE
78 70 6	PP1V8_S0	IN	FUNC_TEST=TRUE
77 6	PP2V5_S0	IN	FUNC_TEST=TRUE
74 73 55 6	PPMCH_CORE_S0	IN	FUNC_TEST=TRUE
73 34 6	PP1V05_S0	IN	FUNC_TEST=TRUE
74 6	PP1V25_S0	IN	FUNC_TEST=TRUE
78 77 70 53 13 6	PP3V3_S0	IN	FUNC_TEST=TRUE
94 78 74 73 72 71 70 6	PP5V_S0	IN	FUNC_TEST=TRUE
76 74 73 53 6	PP12V_S0	IN	FUNC_TEST=TRUE
73 6	PP1V5_S0	IN	FUNC_TEST=TRUE

3 TP'S

"S3" RAILS

78 75 6	PP1V8_S3	IN	FUNC_TEST=TRUE
78 76 75 70 6	PP3V3_S3	IN	FUNC_TEST=TRUE
78 76 75 70 6	PP5V_S3	IN	FUNC_TEST=TRUE
78 75 49 46 25 7	PM_S4_STATE_L	IN	FUNC_TEST=TRUE

3 TP'S

"S5" RAILS

77 75 70 6	PP3V3_S5	IN	FUNC_TEST=TRUE
78 77 76 70 6	PP5V_S5	IN	FUNC_TEST=TRUE
76 75 70 53 6	PP12V_S5	IN	FUNC_TEST=TRUE

5 TP'S

FOR ICT

105 30 16 7	NB_CLK100M_PCIE_N	IN	FUNC_TEST=TRUE
105 30 14 7	FSB_CLK_NB_N	IN	FUNC_TEST=TRUE
16	TP_NB_CFG<13>	IN	FUNC_TEST=TRUE
16	TP_NB_CFG<12>	IN	FUNC_TEST=TRUE
16	TP_NB_CFG<18>	IN	FUNC_TEST=TRUE
16	NB_CFG<19>	IN	FUNC_TEST=TRUE
104 24	PCI_REQ1_L	IN	FUNC_TEST=TRUE
104 24	PCI_REQ2_L	IN	FUNC_TEST=TRUE
105 30 24 7	SB_CLK100M_DMI_N	IN	FUNC_TEST=TRUE
30	TP_CK505_REF1	IN	FUNC_TEST=TRUE
30	TP_CK505_PCI1_CLK	IN	FUNC_TEST=TRUE
40	TP_FW_TCK	IN	FUNC_TEST=TRUE
40	TP_FW_TMS	IN	FUNC_TEST=TRUE
40	TP_FW_TDI	IN	FUNC_TEST=TRUE
40	TP_FW_TDO	IN	FUNC_TEST=TRUE
40	FW_TRST_L	IN	FUNC_TEST=TRUE
40	TP_FW_SM	IN	FUNC_TEST=TRUE
40	TP_FW_SE	IN	FUNC_TEST=TRUE
40	TP_FW_NAND_TREE	IN	FUNC_TEST=TRUE
40	TP_FW_CE	IN	FUNC_TEST=TRUE
103 61	SPI_CE_L<0>	IN	FUNC_TEST=TRUE
103 61	SPI_A_SO_R	IN	FUNC_TEST=TRUE
16	TP_NB_RSVD<12>	IN	FUNC_TEST=TRUE
16	TP_NB_RSVD<11>	IN	FUNC_TEST=TRUE
16	TP_NB_RSVD<13>	IN	FUNC_TEST=TRUE
16	TP_NB_RSVD<10>	IN	FUNC_TEST=TRUE
16 13	NB_CFG<3>	IN	FUNC_TEST=TRUE
16 13	NB_CFG<4>	IN	FUNC_TEST=TRUE
16 13	NB_CFG<5>	IN	FUNC_TEST=TRUE
16 13	NB_CFG<6>	IN	FUNC_TEST=TRUE
16 13	NB_CFG<7>	IN	FUNC_TEST=TRUE
22	TP_LVDS_BKLT_EN	IN	FUNC_TEST=TRUE
103 44 24	ODD_RST_5VTOL_L	IN	FUNC_TEST=TRUE
28 23 7	SB_RTC_RST_L	IN	FUNC_TEST=TRUE
105 30 24 7	SB_CLK100M_DMI_P	IN	FUNC_TEST=TRUE
40 28 7	FW_RESET_L	IN	FUNC_TEST=TRUE
103 61	SPI_SCLK	IN	FUNC_TEST=TRUE
37	ENET_CLK25M_XTALI	IN	FUNC_TEST=TRUE
37	ENET_CLK25M_XTALO	IN	FUNC_TEST=TRUE

NO TEST

16	TP_NB_NC<1>	NO_TEST=TRUE	
16	TP_NB_NC<2>	NO_TEST=TRUE	
16	TP_NB_NC<3>	NO_TEST=TRUE	
16	TP_NB_NC<4>	NO_TEST=TRUE	
16	TP_NB_NC<5>	NO_TEST=TRUE	
28 23	TP_LAN_D2R<2>	NO_TEST=TRUE	
34 28 25	TP_CLINK_WLAN_DATA	NO_TEST=TRUE	
29	TP_CK505_PGMODE	NO_TEST=TRUE	
28	TP_PCI_AD_4	NO_TEST=TRUE	
104 28 24	PCI_SERR_L	NO_TEST=TRUE	

CRITICAL
SC0700 EMI-SPRING CLIP-SM1

CRITICAL
SC0701 EMI-SPRING CLIP-SM1

CRITICAL
SC0702 EMI-SPRING CLIP-SM-K2
BTW DIMMS

CRITICAL
860-0894
SDF0724
SPACER-8P90D1P07H-TH

CRITICAL
SDF0726
HSK-NUT-6.5MM TH
452-0508

CRITICAL
SDF0727
HSK-NUT-6.5MM TH

998-0846 FOR NB HEATSINK

OMIT ZH0722 4R3P25
OMIT ZH0723 4R3P25
OMIT ZH0725 4R3P25

998-0850

OMIT ZH0700 4P75R4
OMIT ZH0701 4P75R4
OMIT ZH0702 4P75R4
OMIT ZH0703 4P75R4

998-0847

OMIT ZH0710 4P25R3P5
OMIT ZH0711 5R3P5-6B
998-1608
OMIT ZH0712 4P25R3P5
OMIT ZH0713 4P25R3P5
OMIT ZH0714 4P25R3P5
OMIT ZH0715 4P25R3P5

998-0847

OMIT ZH0718 4P25R3P5
OMIT ZH0719 4P25R3P5
OMIT ZH0720 4P25R3P5

CRITICAL
860-0895
SDF0717
STDOFF-7P90D15P0H-TH

CRITICAL
860-0895
SDF0721
STDOFF-7P90D15P0H-TH

MISC GROUND VIAS - NEEDED?

ZH500 HOLE-VIA
ZH501 HOLE-VIA
ZH502 HOLE-VIA
ZH503 HOLE-VIA
ZH504 HOLE-VIA
ZH505 HOLE-VIA
ZH506 HOLE-VIA
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ZH526 HOLE-VIA
ZH527 HOLE-VIA
ZH528 HOLE-VIA
ZH529 HOLE-VIA

Functional / ICT Test

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE NONE SHT 7 OF 118

GND RAILS

98 GND_AUDIO_SPKRAMP
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
NET_SPACING_TYPE=GND

CHASSIS GND

GND
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=0V
NET_SPACING_TYPE=GND
MAKE_BASE=TRUE
MAX_NECK_LENGTH=4.1 MM

46 GND_CHASSIS_USB

43 GND_CHASSIS_FIREWIRE
39 GND_CHASSIS_ENET
94 =GND_CHASSIS_DVI

NOTE:
PER EMC REQUIREMENTS, ALL CHASSIS GROUNDS ARE TIED DIRECTLY TO GND

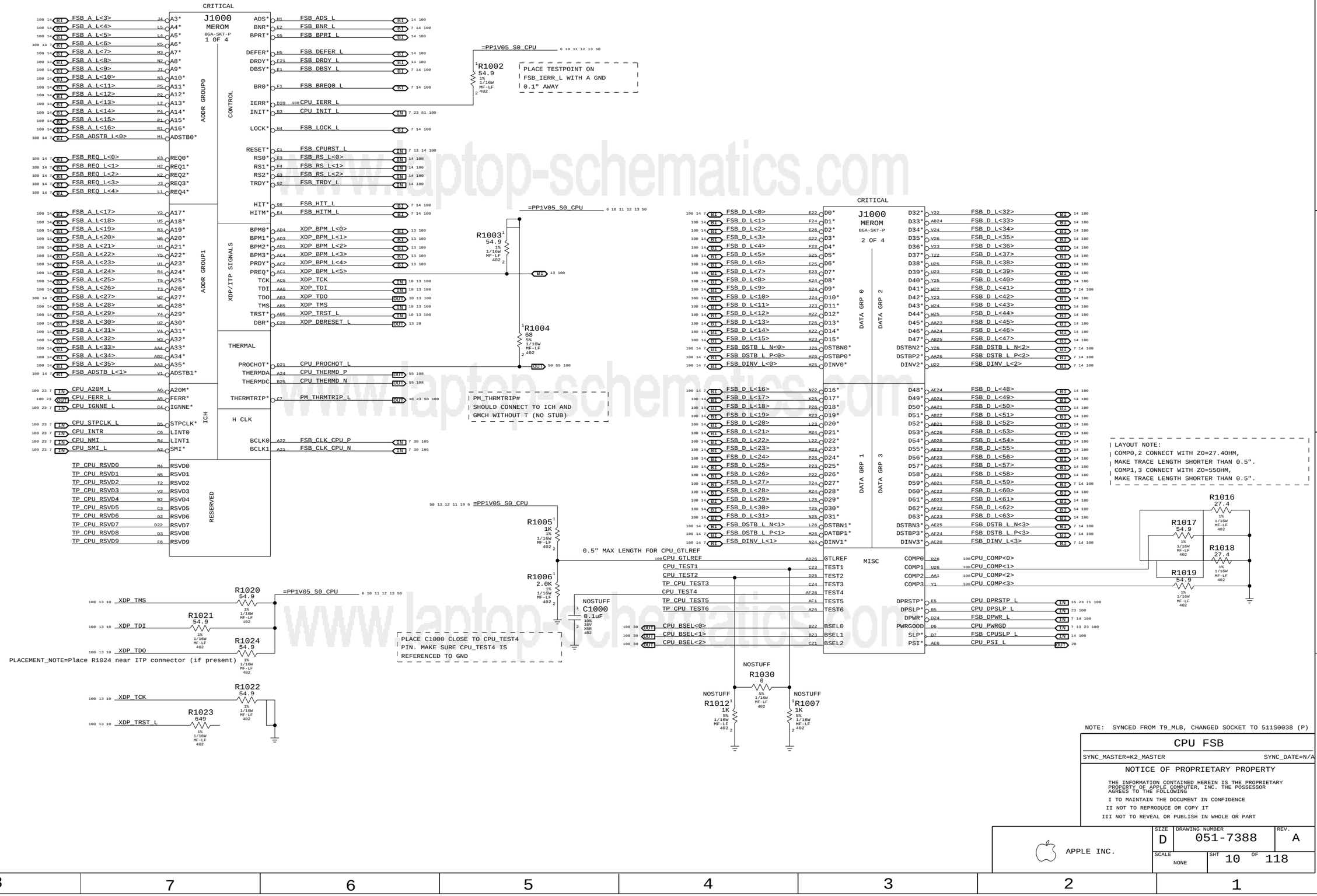
GROUNDING ALIASES

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE NONE SHT 9 OF 118


CRITICAL
J1000
MEROM
BGA-SKT-P
1 OF 4
ADDR GROUP0
ADDR GROUP1
CONTROL
XDP/ITP SIGNALS
THERMAL
H CLK
ICH
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
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FSB_A_L<11>
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FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
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FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_A_L<32>
FSB_A_L<33>
FSB_A_L<34>
FSB_A_L<35>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_RSVD0
TP_CPU_RSVD1
TP_CPU_RSVD2
TP_CPU_RSVD3
TP_CPU_RSVD4
TP_CPU_RSVD5
TP_CPU_RSVD6
TP_CPU_RSVD7
TP_CPU_RSVD8
TP_CPU_RSVD9
ADS*
BNR*
BPRI*
DEFER*
DRDY*
DBSY*
BR0*
IERR*
INIT*
LOCK*
RESET*
RS0*
RS1*
RS2*
TRDY*
HIT*
HITM*
BPM0*
BPM1*
BPM2*
BPM3*
PRDY*
PREQ*
TCK
TDI
TDO
TMS
TRST*
DBR*
PROCHOT*
THERMDA
THERMDC
THERMTRIP*
BCLK0
BCLK1
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
CPU_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
=PP1V05_S0_CPU
R1002 54.9 1% 1/16W MF-LF 402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
R1003 54.9 1% 1/16W MF-LF 402
R1004 68 5% 1/16W MF-LF 402
PM_THRMTRIP# SHOULD CONNECT TO ICH AND GMCH WITHOUT T (NO STUB)
R1005 1K 1% 1/16W MF-LF 402
R1006 2.0K 1% 1/16W MF-LF 402
0.5" MAX LENGTH FOR CPU_GTLREF
NOSTUFF C1000 0.1uF 10% 16V X5R 402
PLACE C1000 CLOSE TO CPU_TEST4 PIN. MAKE SURE CPU_TEST4 IS REFERENCED TO GND
R1020 54.9 1% 1/16W MF-LF 402
R1021 54.9 1% 1/16W MF-LF 402
R1024 54.9 1% 1/16W MF-LF 402
PLACEMENT_NOTE=Place R1024 near ITP connector (if present)
R1022 54.9 1% 1/16W MF-LF 402
R1023 649 1% 1/16W MF-LF 402
CRITICAL
J1000
MEROM
BGA-SKT-P
2 OF 4
DATA GRP 0
DATA GRP 1
DATA GRP 2
DATA GRP 3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
FSB_D_L<6>
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FSB_D_L<8>
FSB_D_L<9>
FSB_D_L<10>
FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTB_L_N<0>
FSB_DSTB_L_P<0>
FSB_DINV_L<0>
FSB_D_L<16>
FSB_D_L<17>
FSB_D_L<18>
FSB_D_L<19>
FSB_D_L<20>
FSB_D_L<21>
FSB_D_L<22>
FSB_D_L<23>
FSB_D_L<24>
FSB_D_L<25>
FSB_D_L<26>
FSB_D_L<27>
FSB_D_L<28>
FSB_D_L<29>
FSB_D_L<30>
FSB_D_L<31>
FSB_DSTB_L_N<1>
FSB_DSTB_L_P<1>
FSB_DINV_L<1>
FSB_D_L<32>
FSB_D_L<33>
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FSB_D_L<35>
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FSB_D_L<44>
FSB_D_L<45>
FSB_D_L<46>
FSB_D_L<47>
FSB_DSTB_L_N<2>
FSB_DSTB_L_P<2>
FSB_DINV_L<2>
FSB_D_L<48>
FSB_D_L<49>
FSB_D_L<50>
FSB_D_L<51>
FSB_D_L<52>
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FSB_D_L<56>
FSB_D_L<57>
FSB_D_L<58>
FSB_D_L<59>
FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTB_L_N<3>
FSB_DSTB_L_P<3>
FSB_DINV_L<3>
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
CPU_GTLREF
CPU_TEST1
CPU_TEST2
TP_CPU_TEST3
CPU_TEST4
TP_CPU_TEST5
TP_CPU_TEST6
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_CPUSLP_L
CPU_PSI_L
NOSTUFF R1030 0
NOSTUFF R1012 1K 5% 1/16W MF-LF 402
NOSTUFF R1007 1K 5% 1/16W MF-LF 402
R1016 27.4 1% 1/16W MF-LF 402
R1017 54.9 1% 1/16W MF-LF 402
R1018 27.4 1% 1/16W MF-LF 402
R1019 54.9 1% 1/16W MF-LF 402
LAYOUT NOTE:
COMP0,2 CONNECT WITH ZO=27.4OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
COMP1,3 CONNECT WITH ZO=55OHM,
MAKE TRACE LENGTH SHORTER THAN 0.5".
NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)
CPU FSB
SYNC_MASTER=K2_MASTER
SYNC_DATE=N/A
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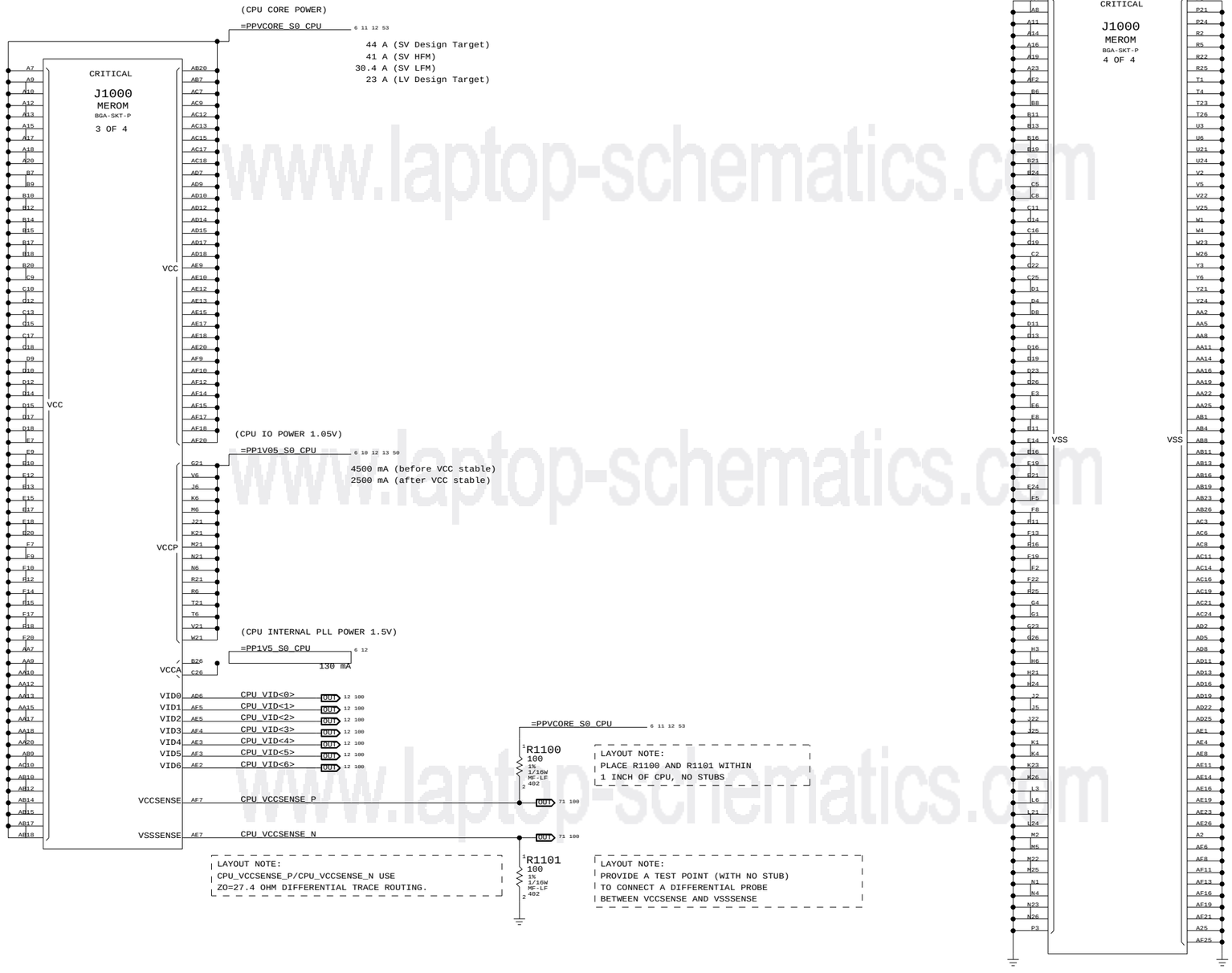
SIZE D
DRAWING NUMBER 051-7388
REV. A
SCALE NONE
SHT 10 OF 118



Current numbers from Merom for Santa Rosa EMTS, doc #20905.

NOTE: SYNCED FROM T9_MLB, CHANGED SOCKET TO 511S0038 (P)

CPU Power & Ground

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

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SCALE	SHT	OF
NONE	11	118

CPU VCORE HF AND BULK DECOUPLING

6X 220UF. 32X 22UF 0805

53 11 6 =PPVCORE_S0_CPU

NOTE: CHANGED TO X5R CAPS TO MATCH PREVIOUS IMACS AND FOR C4

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

NOSTUFF C1200 22UF 20% 6.3V CERM-X5R 805
C1201 C1202 C1203 C1204 C1205 C1206 C1207 C1208 C1209 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE INSIDE SOCKET CAVITY (ON BOTTOMSIDE)

C1210 C1211 C1212 C1213 C1214 C1215 C1216 C1217 C1218 C1219 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET NORTH SIDE (ON TOPSIDE)

C1220 C1221 NOSTUFF C1222 NOSTUFF C1223 NOSTUFF C1224 NOSTUFF C1225 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE NEAR SOCKET SOUTH SIDE (ON TOPSIDE)

C1226 C1227 NOSTUFF C1228 NOSTUFF C1229 C1230 NOSTUFF C1231 — 22UF 20% 6.3V CERM-X5R 805

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CRITICAL NOSTUFF C1250 220UF 20% 2V POLY CASE-D2-SM1
CRITICAL C1251 CRITICAL C1254 CRITICAL C1255 CRITICAL C1252 CRITICAL C1253 — 220UF 20% 2V POLY CASE-D2-SM1

LAYOUT NOTE:
PLACE ON BOTTOMSIDE

CPU VCORE VID CONNECTIONS

Resistors to allow for override of CPU VID
Will probably be removed before production

R1290	0 5% 1/16W MF-LF 402	100 11 CPU_VID<0>	IMVP6_VID<0>	71 100
R1291	0 5% 1/16W MF-LF 402	100 11 CPU_VID<1>	IMVP6_VID<1>	71 100
R1292	0 5% 1/16W MF-LF 402	100 11 CPU_VID<2>	IMVP6_VID<2>	71 100
R1293	0 5% 1/16W MF-LF 402	100 11 CPU_VID<3>	IMVP6_VID<3>	71 100
R1294	0 5% 1/16W MF-LF 402	100 11 CPU_VID<4>	IMVP6_VID<4>	71 100
R1295	0 5% 1/16W MF-LF 402	100 11 CPU_VID<5>	IMVP6_VID<5>	71 100
R1296	0 5% 1/16W MF-LF 402	100 11 CPU_VID<6>	IMVP6_VID<6>	71 100

VCCA (CPU AVdd) DECOUPLING

11 6 =PP1V5_S0_CPU — 1x 10uF, 1x 0.01uF

C1280 10uF 20% 6.3V X5R 603
C1281 0.01UF 10% 16V CERM 402

LAYOUT NOTE:
PLACE C1281 NEAR PIN B26 OF U1000

VCCP (CPU I/O) DECOUPLING

50 13 11 10 6 =PP1V05_S0_CPU — 1X 330UF, 6X 0.1UF 0402

CRITICAL C1235 330UF 20% 6.3V ELEC 6.3X8-SM
C1236 C1237 C1238 C1239 C1240 C1241 — 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C1235 CLOSE TO CPU

CPU Decoupling & VID

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

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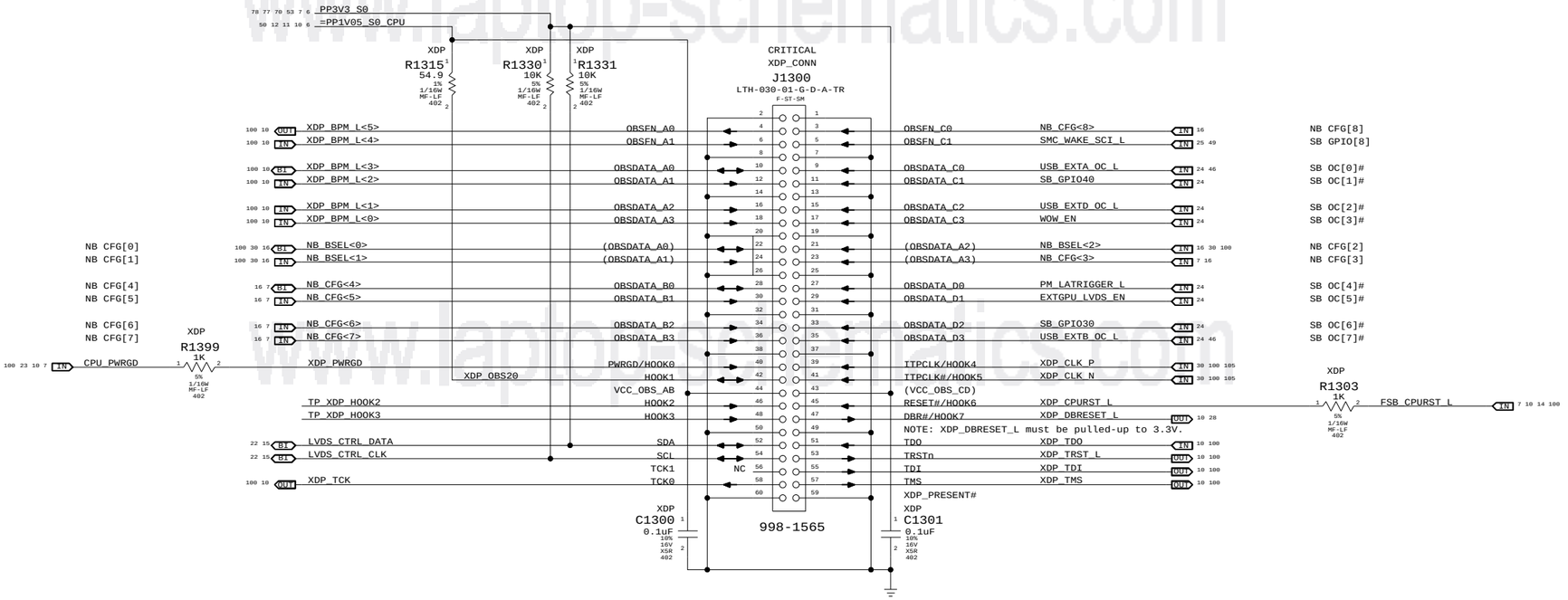
SCALE: NONE	SHT 12 OF 118	

Mini-XDP Connector

NOTE: This is not the standard XDP pinout.

Use with 920-0451 adapter board to support CPU, NB & SB debugging.



Direction of XDP module

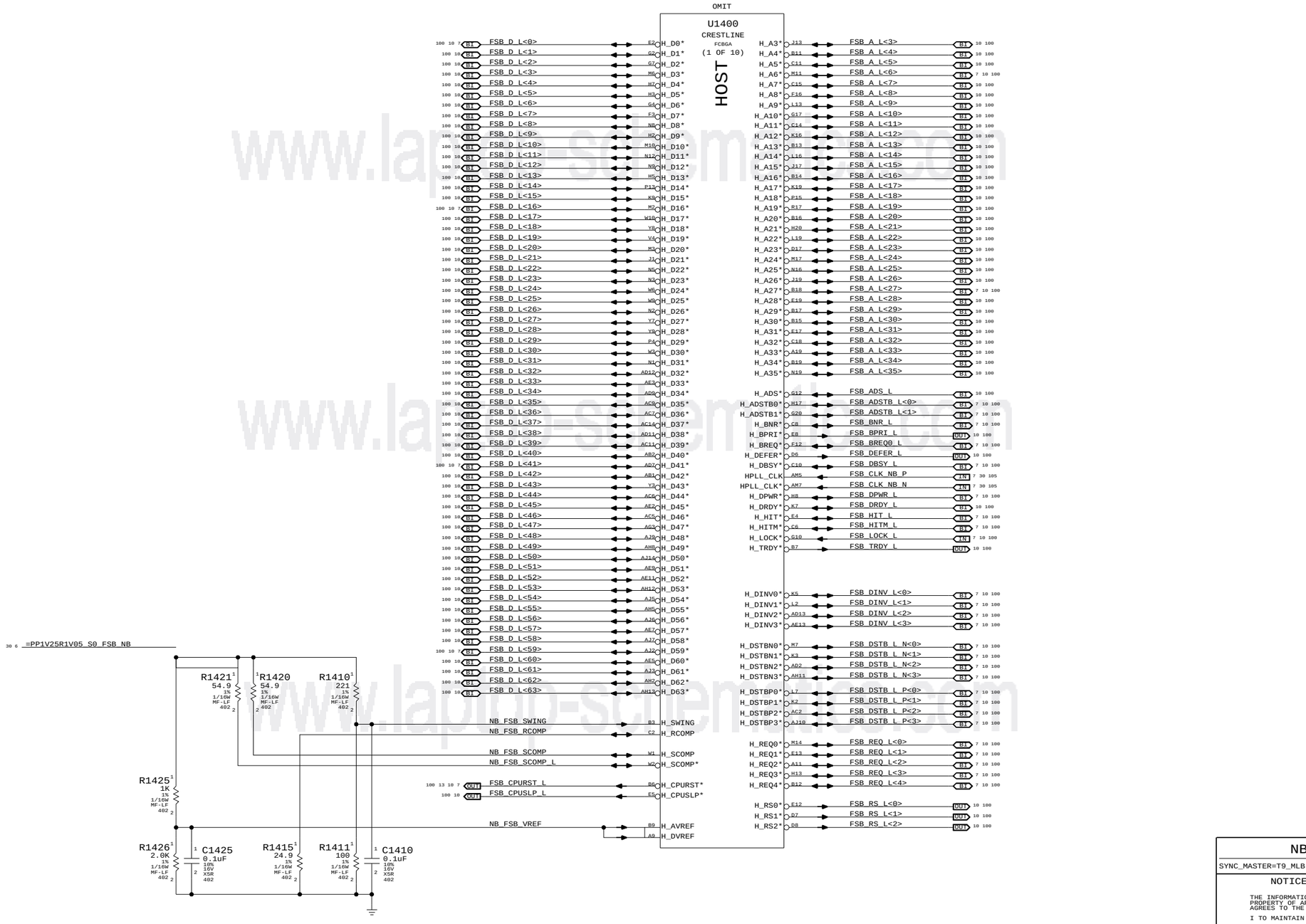
Please avoid any obstructions
on even-numbered side of J1300

eXtended Debug Port (XDP)

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=11/06/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 13 OF 118	



NB CPU Interface

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 14 OF 118	

LVDS Disable

Can leave all signals NC if LVDS is not implemented.
Tie VCC_TX_LVDS and VCCA_LVDS to GND.

If SDVO is used, VCCD_LVDS must remain powered with proper decoupling. Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable / CRT Enable

Tie TVx_DAC and TVx_RTN to GND. Must power all TVDAC rails. VCCA_TVx_DAC and VCCA_DAC_BG can share filtering with VCCA_CRT_DAC.

CRT Disable / TV-Out Enable

Tie R/R#/G/G#/B/B#, HSYNC and VSYNC to GND. All CRT/TVDAC rails must be powered. All rails must be filtered except for VCCA_CRT.

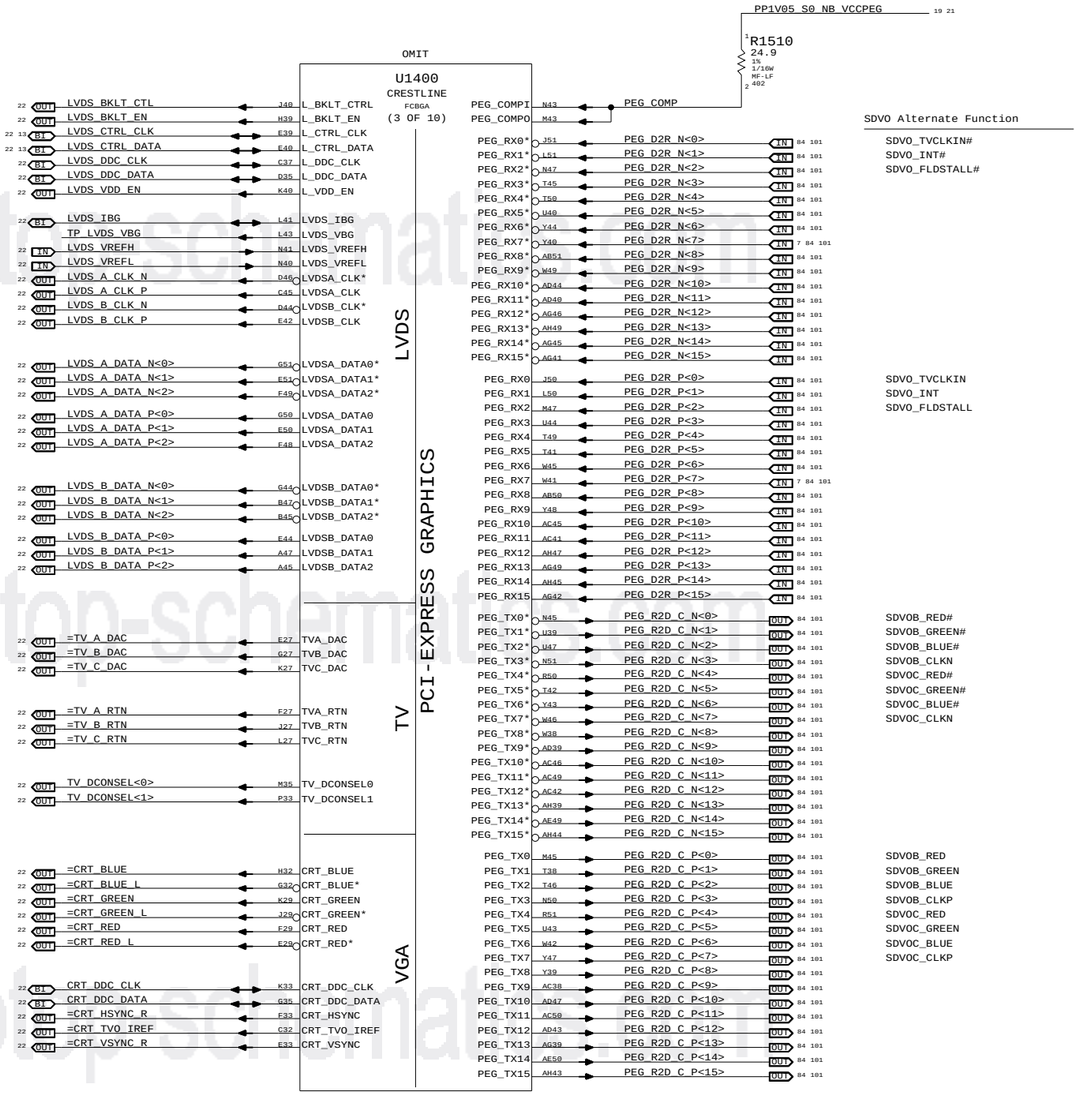
CRT & TV-Out Disable

Tie TVx_DAC, TVx_RTN, R/R#/G/G#/B/B#, HSYNC, VSYNC and CRT_TVO_IREF to GND.
Can tie the following rails to GND:
VCCA_CRT_DAC, VCCA_DAC_BG, VCCA_TVx_DAC, VCCD_CRT, VCCD_QDAC and VCC_SYNC.

NOTE: Must keep VDDC_TVDAC powered and filtered at all times!

Internal Graphics Disable

Follow instructions for LVDS and CRT & TV-Out Disable above.
Can also tie CRT_DDC_*, L_CTRL_*, L_DDC_*, SDVO_CTRL_* and TV_DCONSELx to GND.
Tie DPLL_REF_CLK and DPLL_REF_SSCLK to GND.
Tie DPLL_REF_CLK* and DPLL_REF_SSCLK* to VCC (VCore).
Tie VCCA_DPLLA and VCCA_DPLLB to VCC (VCore).
Tie VCC_AXG and VCC_AXG_NCTF to GND.
Leave GFX_VID<3..0> and GFX_VR_EN as NC.



NB PEG / Video Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 15 OF 118	

NB_CFG<3>	RESERVED
NB_CFG<4>	RESERVED
NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2
NB_CFG<6>	RESERVED
NB_CFG<7>	RESERVED
NB_CFG<8>	RESERVED
NB_CFG<9> PCIe Graphics Lane Reversal	High = Normal Low = Reversed
NB_CFG<10>	RESERVED
NB_CFG<11>	RESERVED
NB_CFG<12>	See Below
NB_CFG<13>	See Below
NB_CFG<14>	RESERVED
NB_CFG<15>	RESERVED
NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled
NB_CFG<17>	RESERVED
NB_CFG<18>	RESERVED
NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal
NB_CFG<20> Concurrent SDVO/PCIe x1	High = Both active Low = Only SDVO or PCIe x16

NB_CFG<13:12>

00 = RESERVED
01 = XOR Mode Enabled
10 = All-Z Mode Enabled
11 = Normal Operation

NB_CFG<5> → NBCFG_DMI_X2 R1655 3.9K 5% 1/16W MF-LF 402

NB_CFG<9> → NBCFG_PEG_REVERSE R1659 3.9K 5% 1/16W MF-LF 402

NB_CFG<16> → NBCFG_DYN_ODT_DISABLE R1666 3.9K 5% 1/16W MF-LF 402

=PP3V3_S0_NB_VCCHV → NBCFG_DMI_REVERSE R1669 3.9K 5% 1/16W MF-LF 402 → NB_CFG<19>

=PP3V3_S0_NB_VCCHV → NBCFG_SDVO_AND_PCIE R1670 3.9K 5% 1/16W MF-LF 402 → NB_CFG<20>

NB CFG<8:0> used for debug access

NB CFG<13:12> require ICT access

=PP3V3_S0_NB_VCCHV → R1630 10K 5% 1/16W MF-LF 402 / R1631 10K 5% 1/16W MF-LF 402

PM_EXTTS_L<0>
PM_EXTTS_L<1>

OMIT

U1400 CRESTLINE FCBGA (2 OF 10)

RSVD
TP_NB_RSVD<1> P36 RSVD1
TP_NB_RSVD<2> P37 RSVD2
TP_NB_RSVD<3> R35 RSVD3
TP_NB_RSVD<4> N35 RSVD4
TP_NB_RSVD<5> AR12 RSVD5
TP_NB_RSVD<6> AR13 RSVD6
TP_NB_RSVD<7> AM12 RSVD7
TP_NB_RSVD<8> AN13 RSVD8
TP_NB_RSVD<9> J12 RSVD9
TP_NB_RSVD<10> AR37 RSVD10
TP_NB_RSVD<11> AM36 RSVD11
TP_NB_RSVD<12> AL36 RSVD12
TP_NB_RSVD<13> AM37 RSVD13
TP_NB_RSVD<14> D20 RSVD14
TP_NB_RSVD<20> H10 RSVD20
TP_NB_RSVD<21> B51 RSVD21
TP_NB_RSVD<22> BJ20 RSVD22
TP_NB_RSVD<23> BK22 RSVD23
TP_NB_RSVD<24> BF19 RSVD24
TP_NB_RSVD<25> BH20 RSVD25
TP_NB_RSVD<26> BK18 RSVD26
TP_NB_RSVD<27> BJ18 RSVD27
TP_MEM_CLKP2 BF23 SM_CK2
TP_MEM_CLKN2 BG23 SM_CK2*
TP_MEM_CLKP5 BC23 SM_CK5
TP_MEM_CLKN5 BD24 SM_CK5*
MEM_A_A<14> BJ29 SA_MA14
MEM_B_A<14> BE24 SB_MA14
TP_NB_RSVD<34> BH39 RSVD34
TP_NB_RSVD<35> AW20 RSVD35
TP_NB_RSVD<36> BK20 RSVD36
TP_LVDS_A_DATAN3 C48 RSVD37
TP_LVDS_A_DATAP3 D47 RSVD38
TP_LVDS_B_DATAN3 B44 RSVD39
TP_LVDS_B_DATAP3 C44 RSVD40
TP_NB_RSVD<41> A35 RSVD41
TP_NB_RSVD<42> B37 RSVD42
TP_NB_RSVD<43> B36 RSVD43
TP_NB_RSVD<44> B34 RSVD44
TP_NB_RSVD<45> C34 RSVD45

CFG
NB_BSEL<0> P27 CFG0
NB_BSEL<1> N27 CFG1
NB_BSEL<2> N24 CFG2
NB_CFG<3> C21 CFG3 IPU
NB_CFG<4> C23 CFG4 IPU
NB_CFG<5> F23 CFG5 IPU
NB_CFG<6> N23 CFG6 IPU
NB_CFG<7> G23 CFG7 IPU
NB_CFG<8> J20 CFG8 IPU
NB_CFG<9> C20 CFG9 IPU
TP_NB_CFG<10> R24 CFG10 IPU
TP_NB_CFG<11> L23 CFG11 IPU
TP_NB_CFG<12> J23 CFG12 IPU
TP_NB_CFG<13> E23 CFG13 IPU
TP_NB_CFG<14> E20 CFG14 IPU
TP_NB_CFG<15> K23 CFG15 IPU
NB_CFG<16> M20 CFG16 IPU
TP_NB_CFG<17> M24 CFG17 IPU
TP_NB_CFG<18> L32 CFG18 IPD
NB_CFG<19> N33 CFG19 IPD
NB_CFG<20> L35 CFG20 IPD

PM
PM_BMBUSY_L G41 PM_BM_BUSY*
CPU_DPRSTP_L L39 PM_DPRSTP*
L36 PM_EXT_TS0*
J36 PM_EXT_TS1*
VR_PWRGOOD_DELAY AW49 PWROK
NB_RESET_L AV20 RSTIN*
PM_THRMTRIP_L N20 THERMTRIP*
PM_DPRSLPVR G36 DPRSLPVR

NC
TP_NB_NC<1> BJ51 NC1
TP_NB_NC<2> BK51 NC2
TP_NB_NC<3> BK50 NC3
TP_NB_NC<4> BL50 NC4
TP_NB_NC<5> BL49 NC5
TP_NB_NC<6> BL3 NC6
TP_NB_NC<7> BL2 NC7
TP_NB_NC<8> BK1 NC8
TP_NB_NC<9> BJ1 NC9
TP_NB_NC<10> E1 NC10
TP_NB_NC<11> A5 NC11
TP_NB_NC<12> C51 NC12
TP_NB_NC<13> B50 NC13
TP_NB_NC<14> A50 NC14
TP_NB_NC<15> A49 NC15
TP_NB_NC<16> BK2 NC16

DDR MUXING
SM_CK0 AV29 → MEM_CLK_P<0>
SM_CK1 BB23 → MEM_CLK_P<1>
SM_CK3 BA25 → MEM_CLK_P<3>
SM_CK4 AV23 → MEM_CLK_P<4>
SM_CK0* AW30 → MEM_CLK_N<0>
SM_CK1* BA23 → MEM_CLK_N<1>
SM_CK3* AW25 → MEM_CLK_N<3>
SM_CK4* AW23 → MEM_CLK_N<4>
SM_CKE0 BE29 → MEM_CKE<0>
SM_CKE1 AY32 → MEM_CKE<1>
SM_CKE3 BD39 → MEM_CKE<3>
SM_CKE4 BG37 → MEM_CKE<4>
SM_CS0* BG20 → MEM_CS_L<0>
SM_CS1* BK16 → MEM_CS_L<1>
SM_CS2* BG16 → MEM_CS_L<2>
SM_CS3* BE13 → MEM_CS_L<3>
SM_ODT0 BH18 → MEM_ODT<0>
SM_ODT1 BJ15 → MEM_ODT<1>
SM_ODT2 BJ14 → MEM_ODT<2>
SM_ODT3 BE16 → MEM_ODT<3>
SM_RCOMP BL15 → MEM_RCOMP
SM_RCOMP* BK14 → MEM_RCOMP_L
SM_RCOMP_VOH BK31 → MEM_RCOMP_VOH
SM_RCOMP_VOL BL31 → MEM_RCOMP_VOL
SM_VREF0 AR49 ← =PP0V9_S3M_MEM_NBVREFA
SM_VREF1 AW4 ← =PP0V9_S3M_MEM_NBVREFB

CLK
DPLL_REF_CLK B42 ← =NB_CLK96M_DOT_P
DPLL_REF_CLK* C42 ← =NB_CLK96M_DOT_N
DPLL_REF_SSCLK H48 ← =NB_CLK100M_DPLLSS_P
DPLL_REF_SSCLK* H47 ← =NB_CLK100M_DPLLSS_N
PEG_CLK K44 ← NB_CLK100M_PCIE_P
PEG_CLK* K45 ← NB_CLK100M_PCIE_N
Clk used for PEG and DMI

DMI
DMI_RXN0 AN47 ← DMI_S2N_N<0>
DMI_RXN1 AJ38 ← DMI_S2N_N<1>
DMI_RXN2 AN42 ← DMI_S2N_N<2>
DMI_RXN3 AN46 ← DMI_S2N_N<3>
DMI_RXP0 AM47 ← DMI_S2N_P<0>
DMI_RXP1 AJ39 ← DMI_S2N_P<1>
DMI_RXP2 AN41 ← DMI_S2N_P<2>
DMI_RXP3 AN45 ← DMI_S2N_P<3>
DMI_TXN0 AJ46 → DMI_N2S_N<0>
DMI_TXN1 AJ41 → DMI_N2S_N<1>
DMI_TXN2 AM40 → DMI_N2S_N<2>
DMI_TXN3 AM44 → DMI_N2S_N<3>
DMI_TXP0 AJ47 → DMI_N2S_P<0>
DMI_TXP1 AJ42 → DMI_N2S_P<1>
DMI_TXP2 AM39 → DMI_N2S_P<2>
DMI_TXP3 AM43 → DMI_N2S_P<3>

GRAPHICS VID
GFX_VID0 E35 → GFX_VID<0>
GFX_VID1 A39 → GFX_VID<1>
GFX_VID2 C38 → GFX_VID<2>
GFX_VID3 B39 → GFX_VID<3>
GFX_VR_EN E36 → =GFX_VR_EN

MISC
SDVO_CTRL_CLK H35 → SDVO_CTRLCLK
SDVO_CTRL_DATA K36 → SDVO_CTRLDATA
CLKREQ* G39 → NB_CLKREQ_L
ICH_SYNC* G40 → NB_SB_SYNC_L
TEST1 A37 → NB_TEST1
TEST2 R32 → NB_TEST2

ME
CL_CLK AM49 → CLINK_NB_CLK
CL_DATA AK50 → CLINK_NB_DATA
CL_PWROK AT43 → =NB_CLINK_MPWROK
CL_RST* AN49 → CLINK_NB_RESET_L
CL_VREF AM50 ← NB_CLINK_VREF

22 21 18 6 =PP1V8_S3M_MEM_NB
R1610 20 1% 1/16W MF-LF 402
R1620 1K 1% 1/16W MF-LF 402
C1623 0.01UF 10% 16V CERM 402
C1622 2.2UF 20% 6.3V CERM1 603
R1622 3.01K 1% 1/16W MF-LF 402
R1611 20 1% 1/16W MF-LF 402
C1625 0.01UF 10% 16V CERM 402
C1624 2.2UF 20% 6.3V CERM1 603
R1624 1K 1% 1/16W MF-LF 402
C1615 0.1uF 20% 10V CERM 402
C1616 0.1uF 20% 10V CERM 402

PP1V25_S0M_NB_VCCAXD
R1640 1K 1% 1/16W MF-LF 402
C1640 0.1uF 20% 10V CERM 402
R1641 392 1% 1/16W MF-LF 402

R1691 20K 5% 1/16W MF-LF 402
R1690 0 5% 1/16W MF-LF 402

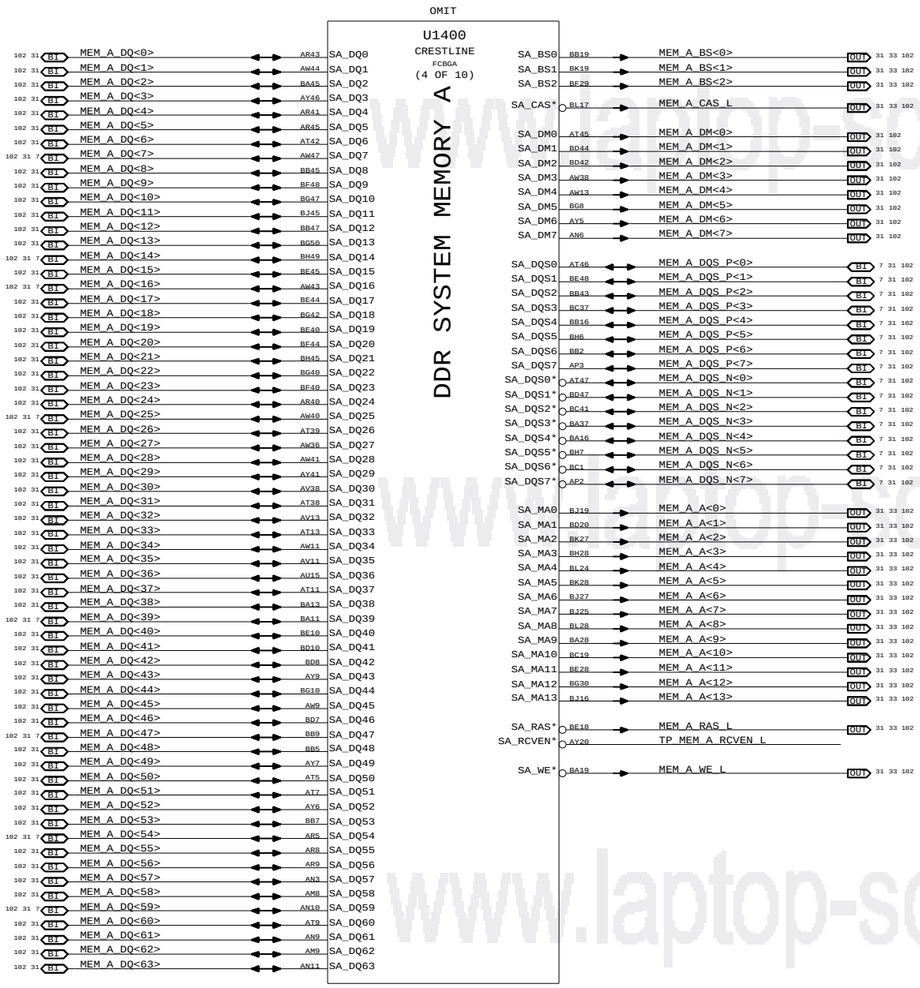
NOTE: GMCH CL_PWROK input must be PWRGD signal for PP3V3_S0M, PP3V3_S0MWOL, PP1V8_S3M, PP1V25_S0M, PP1V05_S0M, PP0V9_S3M and PP0V9_S0M.
If ME/AMT is not used, short CL_PWROK to PWROK.

NB Misc Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=01/21/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 16 OF 118	



NB DDR2 Interfaces

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
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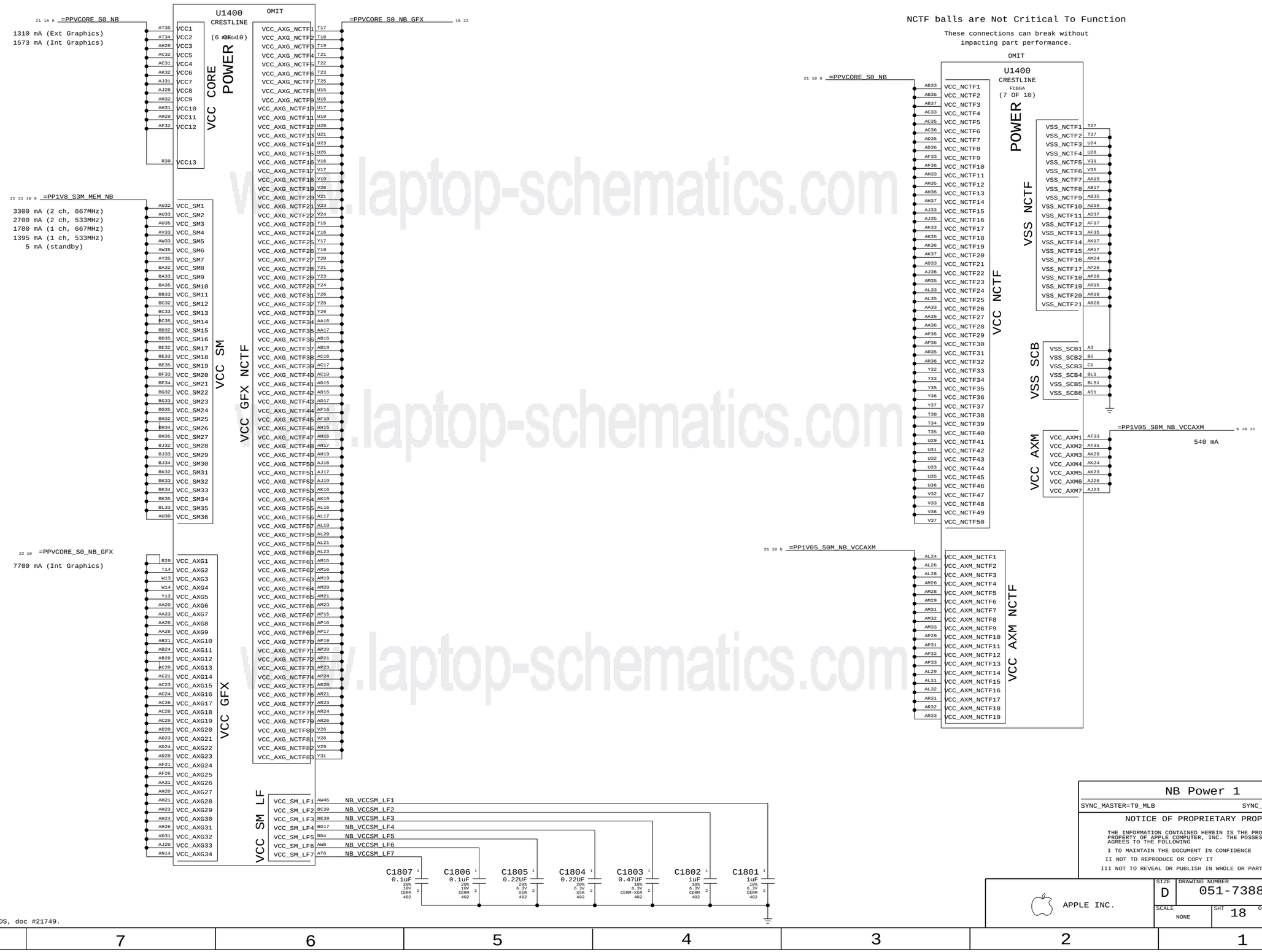
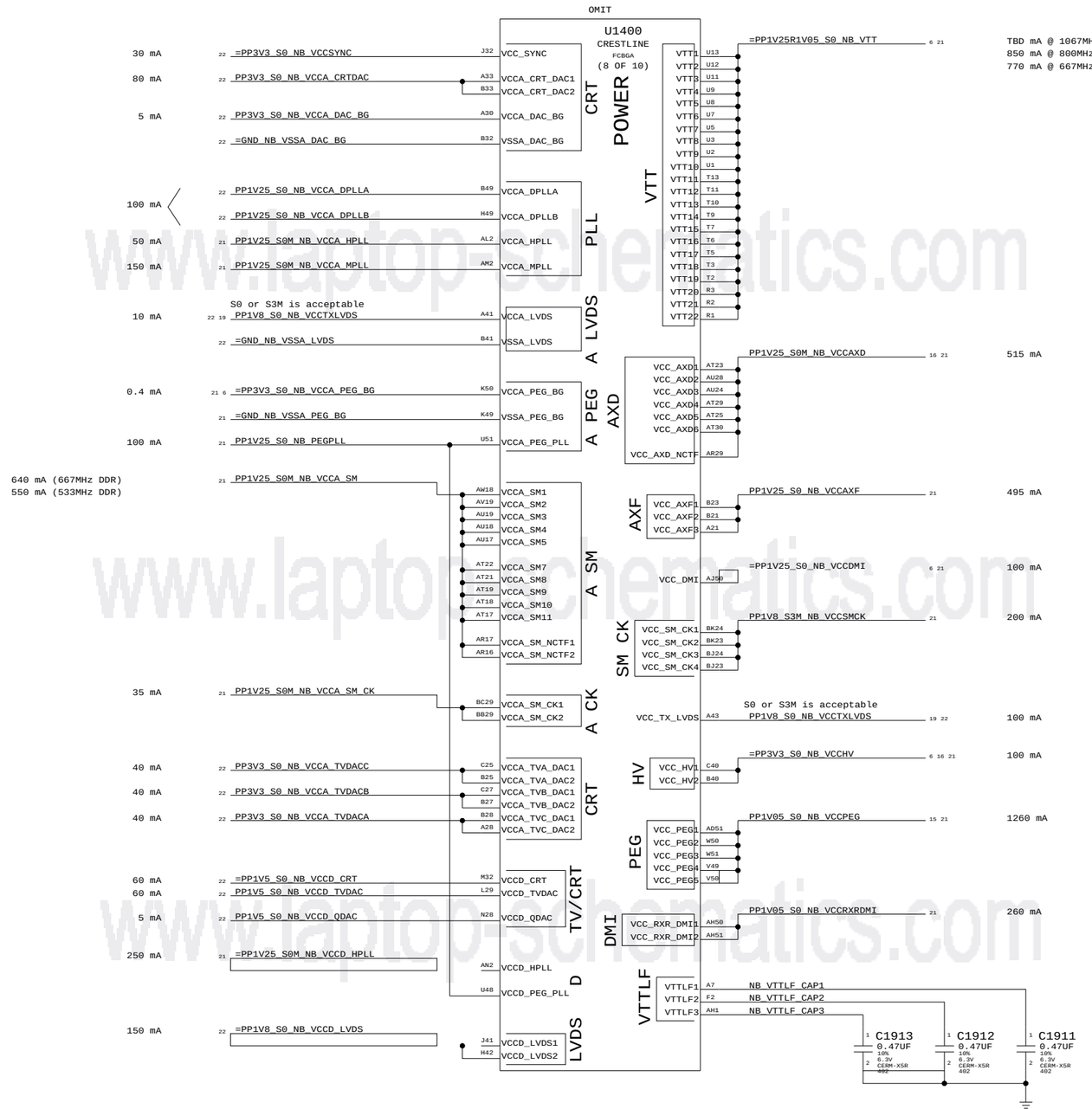
SCALE NONE SHT 17 OF 118





Current numbers from Crestline EDS, doc #21749.

NB Power 2

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 19 OF 118	

OMIT

U1400
CRESTLINE
FCBGA
(9 OF 10)
VSS

A13	VSS1	VSS100	AW24
A15	VSS2	VSS101	AW29
A17	VSS3	VSS102	AW32
A24	VSS4	VSS103	AW5
AA21	VSS5	VSS104	AW7
AA24	VSS6	VSS105	AY10
AA29	VSS7	VSS106	AY24
AB20	VSS8	VSS107	AY37
AB23	VSS9	VSS108	AY42
AB26	VSS10	VSS109	AY43
AB28	VSS11	VSS110	AY45
AB31	VSS12	VSS111	AY47
AC10	VSS13	VSS112	AY50
AC13	VSS14	VSS113	B10
AC3	VSS15	VSS114	B20
AC39	VSS16	VSS115	B24
AC43	VSS17	VSS116	B29
AC47	VSS18	VSS117	B30
AD1	VSS19	VSS118	B35
AD21	VSS20	VSS119	B38
AD26	VSS21	VSS120	B43
AD29	VSS22	VSS121	B46
AD3	VSS23	VSS122	B5
AD41	VSS24	VSS123	B8
AD45	VSS25	VSS124	BA1
AD49	VSS26	VSS125	BA17
AD5	VSS27	VSS126	BA18
AD50	VSS28	VSS127	BA2
AD8	VSS29	VSS128	BA24
AE10	VSS30	VSS129	BB12
AE14	VSS31	VSS130	BB25
AE6	VSS32	VSS131	BB40
AF20	VSS33	VSS132	BB44
AF23	VSS34	VSS133	BB49
AF24	VSS35	VSS134	BB8
AF31	VSS36	VSS135	BC16
AG2	VSS37	VSS136	BC24
AG38	VSS38	VSS137	BC25
AG43	VSS39	VSS138	BC36
AG47	VSS40	VSS139	BC40
AG50	VSS41	VSS140	BC51
AH3	VSS42	VSS141	BD13
AH40	VSS43	VSS142	BD2
AH41	VSS44	VSS143	BD28
AH7	VSS45	VSS144	BD45
AH9	VSS46	VSS145	BD48
AJ11	VSS47	VSS146	BD5
AJ13	VSS48	VSS147	BE1
AJ21	VSS49	VSS148	BE19
AJ24	VSS50	VSS149	BE23
AJ29	VSS51	VSS150	BE30
AJ32	VSS52	VSS151	BE42
AJ43	VSS53	VSS152	BE51
AJ45	VSS54	VSS153	BE8
AJ49	VSS55	VSS154	BF12
AK20	VSS56	VSS155	BF16
AK21	VSS57	VSS156	BF36
AK26	VSS58	VSS157	BG19
AK28	VSS59	VSS158	BG2
AK31	VSS60	VSS159	BG24
AK51	VSS61	VSS160	BG29
AL1	VSS62	VSS161	BG39
AM11	VSS63	VSS162	BG48
AM13	VSS64	VSS163	BG5
AM3	VSS65	VSS164	BG51
AM4	VSS66	VSS165	BH17
AM41	VSS67	VSS166	BH30
AM45	VSS68	VSS167	BH44
AN1	VSS69	VSS168	BH46
AN38	VSS70	VSS169	BH8
AN39	VSS71	VSS170	BJ11
AN43	VSS72	VSS171	BJ13
AN5	VSS73	VSS172	BJ38
AN7	VSS74	VSS173	BJ4
AP4	VSS75	VSS174	BJ42
AP48	VSS76	VSS175	BJ46
AP50	VSS77	VSS176	BK15
AR11	VSS78	VSS177	BK17
AR2	VSS79	VSS178	BK25
AR39	VSS80	VSS179	BK29
AR44	VSS81	VSS180	BK36
AR47	VSS82	VSS181	BK40
AR7	VSS83	VSS182	BK44
AT10	VSS84	VSS183	BK6
AT14	VSS85	VSS184	BK8
AT41	VSS86	VSS185	BL11
AT49	VSS87	VSS186	BL13
AU1	VSS88	VSS187	BL19
AU23	VSS89	VSS188	BL22
AU29	VSS90	VSS189	BL37
AU3	VSS91	VSS190	BL47
AU36	VSS92	VSS191	C12
AU49	VSS93	VSS192	C16
AU51	VSS94	VSS193	C19
AV39	VSS95	VSS194	C28
AV48	VSS96	VSS195	C29
AW1	VSS97	VSS196	C33
AW12	VSS98	VSS197	C36
AW16	VSS99	VSS198	C41

OMIT

U1400
CRESTLINE
FCBGA
(10 OF 10)
VSS

C46	VSS199	VSS287	W11
C50	VSS200	VSS288	W39
C7	VSS201	VSS289	W43
D13	VSS202	VSS290	W47
D24	VSS203	VSS291	W5
D3	VSS204	VSS292	W7
D32	VSS205	VSS293	Y13
D39	VSS206	VSS294	Y2
D45	VSS207	VSS295	Y41
D49	VSS208	VSS296	Y45
E10	VSS209	VSS297	Y49
E16	VSS210	VSS298	Y5
E24	VSS211	VSS299	Y50
E28	VSS212	VSS300	Y11
E32	VSS213	VSS301	P29
E47	VSS214		
F19	VSS215		
F36	VSS216	TDE_SENSE	VSS302 T29
F4	VSS217		
F40	VSS218		
F50	VSS219	TDE_FORCE	VSS303 T31
G1	VSS220		
G13	VSS221		
G16	VSS222	TDB_FORCE	VSS304 T33
G19	VSS223		
G24	VSS224		
G28	VSS225	TDB_SENSE	VSS305 R28
G29	VSS226		
G33	VSS227		
G42	VSS228		
G45	VSS229	VSS306	AA32
G48	VSS230	VSS307	AB32
G8	VSS231	VSS308	AD32
H24	VSS232	VSS309	AF28
H28	VSS233	VSS310	AF29
H4	VSS234	VSS311	AT27
H45	VSS235	VSS312	AV25
J11	VSS236	VSS313	H50
J16	VSS237		
J2	VSS238		
J24	VSS239		
J28	VSS240		
J33	VSS241		
J35	VSS242		
J39	VSS243		
K12	VSS245		
K47	VSS246		
K8	VSS247		
L1	VSS248		
L17	VSS249		
L20	VSS250		
L24	VSS251		
L28	VSS252		
L3	VSS253		
L33	VSS254		
L49	VSS255		
M28	VSS256		
M42	VSS257		
M46	VSS258		
M49	VSS259		
M5	VSS260		
M50	VSS261		
M9	VSS262		
N11	VSS263		
N14	VSS264		
N17	VSS265		
N29	VSS266		
N32	VSS267		
N36	VSS268		
N39	VSS269		
N44	VSS270		
N49	VSS271		
N7	VSS272		
P19	VSS273		
P2	VSS274		
P23	VSS275		
P3	VSS276		
P50	VSS277		
R49	VSS278		
T39	VSS279		
T43	VSS280		
T47	VSS281		
U41	VSS282		
U45	VSS283		
U50	VSS284		
V2	VSS285		
V3	VSS286		

Crestline Thermal Diode Pins

Mainly for investigation. If not used, alias these nets directly to GND.

TDE_SENSE =NB_TDE_SENSE 55

NOTE: TDE = _P

TDE_FORCE =NB_TDE_FORCE 55

TDB_FORCE =NB_TDB_FORCE 55

NOTE: TDB = _N

TDB_SENSE =NB_TDB_SENSE 55

NB Grounds

SYNC_MASTER=T9_MLB SYNC_DATE=10/30/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 20 OF 118	

GMCH Core Power

=PPVCORE_S0_NB

1573mA (Int Graphics)
1310mA (Ext Graphics)

C2100 330UF 20% 6.3V ELEC 6.3X8-SM
C2101 22uF 20% 6.3V CERM 805
C2102 0.22uF 20% 6.3V X5R 402
C2103 0.22uF 20% 6.3V X5R 402
C2104 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place in GMCH cavity

WF: Matanzas has 2-pin 270uF bulk cap

GMCH ME Core Power

=PP1V05_S0M_NB_VCCAXM

540 mA

C2110 22uF 20% 6.3V CERM 805
C2111 0.22uF 20% 6.3V X5R 402
C2112 0.22uF 20% 6.3V X5R 402
C2113 0.1uF 20% 10V CERM 402
C2114 0.1uF 20% 10V CERM 402
C2115 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place in GMCH cavity

GMCH FSB I/O Rail

=PP1V25R1V05_S0_NB_VTT

850 mA (800MHz FSB)
770 mA (667MHz FSB)

C2120 330UF 20% 6.3V ELEC 6.3X8-SM
C2121 4.7uF 20% 6.3V CERM 603
C2122 4.7uF 20% 6.3V CERM 603
C2123 2.2uF 20% 6.3V CERM1 603
C2124 0.47UF 10% 6.3V CERM-X5R 402

PLACEMENT_NOTE=Place close to U1400

WF: Matanzas has 270uF

GMCH Memory I/O Rail

=PP1V8_S3M_MEM_NB

3300 mA (2ch 667MHz)
2700 mA (2ch 533MHz)
1700 mA (1ch 667MHz)
1395 mA (1ch 533MHz)
5 mA (standby)

C2130 330UF 20% 6.3V ELEC 6.3X8-SM
C2135 0.1uF 20% 10V CERM 402
C2131 22uF 20% 6.3V CERM 805
C2132 22uF 20% 6.3V CERM 805

PLACEMENT_NOTE=Place close to U1400

WF: "Place where LVDS and DDR2 taps." (C2125)

Placeholder for 3.9nH, 1A, 32mOhm

=PP1V25_S0M_NB_VCCA

675 mA (667MHz DDR2)
585 mA (533MHz DDR2)

R2141 0 5% 1/10W MF-LF 603
C2140 330UF 20% 6.3V ELEC 6.3X8-SM
NO STUFF C2141 22uF 20% 6.3V CERM 805
C2142 22uF 20% 6.3V CERM 805
C2143 4.7UF 20% 6.3V CERM 603
C2144 1UF 10% 10V X5R 402-1

PP1V25_S0M_NB_VCCA_SM
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

640 mA (667MHz DDR2)
550 mA (533MHz DDR2)

Placeholder for 2.2nH, 1.4A, 17mOhm

R2145 0 5% 1/10W MF-LF 603
C2145 22uF 20% 6.3V CERM 805
NO STUFF C2146 2.2uF 20% 6.3V CERM1 603
C2148 0.1uF 20% 10V CERM 402

PP1V25_S0M_NB_VCCA_SM_CK
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

35 mA

Placeholder for 5.6nH, 0.9A, 45mOhm max

=PP1V25_S0M_NB_VCC

515 mA

NO STUFF L2150 FERR-120-OHM-0.2A 0603
R2150 0 5% 1/10W MF-LF 603

NO STUFF C2150 22uF 20% 6.3V CERM 805
C2151 1UF 10% 10V X5R 402-1

PP1V25_S0M_NB_VCCAXD
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

515 mA

100 mA =PP3V3_S0_NB_VCCHV
100 mA =PP1V25_S0_NB_VCCDMI

C2160 0.1uF 20% 10V CERM 402
C2161 0.1uF 20% 10V CERM 402

=PP3V3_S0_NB_VCCA_PEG_BG

C2165 0.1uF 20% 10V CERM 402

0.4 mA

=GND_NB_VSSA_PEG_BG

Layout Note: Route to caps, then GND

=PP1V25_S0_NB_VCC

495 mA

R2170 0 5% 1/10W MF-LF 603

PP1V25_S0_NB_VCCAXF
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

495 mA

C2170 10uF 20% 6.3V X5R 603
C2171 1UF 10% 10V X5R 402-1

=PP1V25_S0_NB_PCIE

1520 mA

L2173 91NH 1210 CRITICAL

PP1V05_S0_NB_VCCPEG
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
MAKE_BASE=TRUE

1260 mA

Layout Note: Place L and C close to MCH

C2173 220UF 20% 16V ELEC SM-CASE-C1
C2174 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

PP1V05_S0_NB_VCCRXRDMI
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V

260 mA

C2177 10uF 20% 6.3V X5R 603

Layout Note: 10uF caps should be close to MCH on opposite side.

=PP1V25_S0M_NB_PLL

450 mA

L2181 FERR-120-OHM-0.2A 0603

C2181 22UF 20% 6.3V CERM 805

L2183 FERR-120-OHM-0.2A 0603

R2183 0.51 1% 1/10W MF-LF 402

C2183 22UF 20% 6.3V CERM 805

PP1V25_S0M_NB_MPLL_RC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

=PP1V25_S0M_NB_VCCD_HPLL

250 mA

C2180 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2180 by U1400.AN2

PP1V25_S0M_NB_VCCA_HPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

50 mA

C2182 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2182 by U1400.AL2

PP1V25_S0M_NB_VCCA_MPLL
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

150 mA

C2184 0.1uF 20% 10V CERM 402

PLACEMENT_NOTE=Place C2184 by U1400.AM2

=PP1V25_S0_NB_FOLLOW

D2185 SOT23 BAT54E3

PP3V3_S0_NB1V05_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

R2185 10 1% 1/16W MF-LF 402

=PP3V3_S0_NB_FOLLOW

BOMOPTION=CR_E

=PPVCORE_S0_NB_FOLLOW

D2186 SOT23 BAT54E3

PP3V3_S0_NBCORE_FOLLOW_R
MIN_LINE_WIDTH=0.4 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=3.3V

BOMOPTION=CR_E

R2186 10 1% 1/16W MF-LF 402

NOTE: This follower is redundant if VCORE is always 1.05V.

=PP1V25_S0_NB_PLL

100 mA

L2190 FERR-220-OHM 0805

R2190 1.1 1% 1/16W MF-LF 402

C2191 0.1uF 20% 10V CERM 402

PP1V25_S0_NB_PEGPLL
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

100 mA

C2192 0.1uF 20% 10V CERM 402

PP1V25_S0_NB_PEGPLL_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.25V

C2190 10uF 20% 6.3V X5R 603

=PP1V8_S3M_NB_VCC

200 mA

L2195 1.0UH-220MA-0.12-OHM 0805

R2195 1.1 1% 1/16W MF-LF 402

C2196 22uF 20% 6.3V CERM 805

PP1V8_S3M_NB_VCCSMCK
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

200 mA

C2197 0.1uF 20% 10V CERM 402

PP1V8_S3M_NB_VCCSMCK_RC
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V

C2195 10uF 20% 6.3V X5R 603

NOTE:
SYNCED FROM T9_MLB_NOME ON 10/31/06
CHANGED C2100,20,30,40,73 TO ELEC

NB Standard Decoupling

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 21 OF 118	

Current numbers from Crestline EDS, doc #21749.

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
P. 227-228 TABLE 95

15	LVDS_BKLT_CTL	TRUE	TP_LVDS_BKLT_CTL	
15	LVDS_BKLT_EN	TRUE	TP_LVDS_BKLT_EN	7
15 13	LVDS_CTRL_CLK			
15 13	LVDS_CTRL_DATA			
15	LVDS_DDC_CLK			
15	LVDS_DDC_DATA			
15	LVDS_VDD_EN	TRUE	TP_LVDS_VDD_EN	
15	LVDS_IBG	TRUE	TP_LVDS_IBG	
15	LVDS_VREFH	TRUE	TP_LVDS_VREFH	
15	LVDS_VREFL	TRUE	TP_LVDS_VREFL	
15	LVDS_A_CLK_N	TRUE	TP_LVDS_A_CLK_N	
15	LVDS_A_CLK_P	TRUE	TP_LVDS_A_CLK_P	
15	LVDS_B_CLK_N	TRUE	TP_LVDS_B_CLK_N	
15	LVDS_B_CLK_P	TRUE	TP_LVDS_B_CLK_P	
15	LVDS_A_DATA_N<0>	TRUE	TP_LVDS_A_DATA_N<0>	
15	LVDS_A_DATA_N<1>	TRUE	TP_LVDS_A_DATA_N<1>	
15	LVDS_A_DATA_N<2>	TRUE	TP_LVDS_A_DATA_N<2>	
15	LVDS_A_DATA_P<0>	TRUE	TP_LVDS_A_DATA_P<0>	
15	LVDS_A_DATA_P<1>	TRUE	TP_LVDS_A_DATA_P<1>	
15	LVDS_A_DATA_P<2>	TRUE	TP_LVDS_A_DATA_P<2>	
15	LVDS_B_DATA_N<0>	TRUE	TP_LVDS_B_DATA_N<0>	
15	LVDS_B_DATA_N<1>	TRUE	TP_LVDS_B_DATA_N<1>	
15	LVDS_B_DATA_N<2>	TRUE	TP_LVDS_B_DATA_N<2>	
15	LVDS_B_DATA_P<0>	TRUE	TP_LVDS_B_DATA_P<0>	
15	LVDS_B_DATA_P<1>	TRUE	TP_LVDS_B_DATA_P<1>	
15	LVDS_B_DATA_P<2>	TRUE	TP_LVDS_B_DATA_P<2>	
15	=TV_A_DAC			
15	=TV_B_DAC			
15	=TV_C_DAC			
15	=TV_A_RTN			
15	=TV_B_RTN			
15	=TV_C_RTN			
15	TV_DCONSEL<0>			
15	TV_DCONSEL<1>			
15	=CRT_BLUE			
15	=CRT_BLUE_L			
15	=CRT_GREEN			
15	=CRT_GREEN_L			
15	=CRT_RED			
15	=CRT_RED_L			
15	CRT_DDC_CLK			
15	CRT_DDC_DATA			
15	=CRT_HSYNC_R			
15	=CRT_TVO_IREF			
15	=CRT_VSYNC_R			
16	=NB_CLK96M_DOT_P			
16	=NB_CLK96M_DOT_N			
16	=NB_CLK100M_DPLLSS_P			
16	=NB_CLK100M_DPLLSS_N			
16	SDVO_CTRLCLK			
16	SDVO_CTRLDATA			
16	GFX_VID<1>	TRUE	TP_GFX_VID<1>	
16	GFX_VID<2>	TRUE	TP_GFX_VID<2>	
16	GFX_VID<3>	TRUE	TP_GFX_VID<3>	
16	GFX_VID<4>	TRUE	TP_GFX_VID<4>	
16	=GFX_VR_EN	TRUE	TP_GFX_VR_EN	

NOTE:
SANTA ROSA DESIGN GUIDE REV 1.5
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	PP1V25_S0_NB_VCCA_DPLLA	19	
	PP1V25_S0_NB_VCCA_DPLLB	19	
	=PP1V5_S0_NB_VCCD_CRT	19	
	PP1V5_S0_NB_VCCD_QDAC	19	
	=PPVCORE_S0_NB_GFX	18	
	PP3V3_S0_NB_VCCA_CRTDAC	19	
	PP3V3_S0_NB_VCCA_TVDACA	19	
	PP3V3_S0_NB_VCCA_TVDACB	19	
	PP3V3_S0_NB_VCCA_TVDACC	19	
	PP3V3_S0_NB_VCCA_DAC_BG	19	
	=GND_NB_VSSA_DAC_BG	19	
	PP1V8_S0_NB_VCCTXLVDS	19	
TP_NB_VSSA_LVDS TRUE	=GND_NB_VSSA_LVDS	19	
	=PP1V8_S0_NB_VCCD_LVDS	19	
	=PP3V3_S0_NB_VCCSYNC	19	

NOTE:
SANTA ROSA PLATFORM P180 FIG 119 - NC
ALSO CONFIRMED WITH INTEL

16 =NB_CLINK_MPWROK	TRUE	VR_PWRGOOD_DELAY	7 16 70 71

VCCD_TVDAC ALSO POWERS INTERNAL THERMAL SENSORS.

6 =PP1V5_S0_NB_TVDAC
65 mA

CRITICAL
C2201
22000pF-1000mA
16V
NPM1B
PP1V5_S0_NB_VCCD_TVDAC 19
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
60 mA

C2213
10uF
20%
6.3V
X5R
603

C2200
0.1uF
20%
10V
CERM
402

Layout Note:
THESE CAPS SHOULD BE
within 6.35 mm of NB edge

21 18 16 6 =PP1V8_S3M_MEM_NB

R2200 1K 5% 1/16W MF-LF 402
R2202 1K 5% 1/16W MF-LF 402
R2201 1K 5% 1/16W MF-LF 402
R2203 1K 5% 1/16W MF-LF 402

PP0V9_S3M_MEM_NBVREFA — =PP0V9_S3M_MEM_NBVREFA 7 16
VOLTAGE=0.9V TRUE
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM

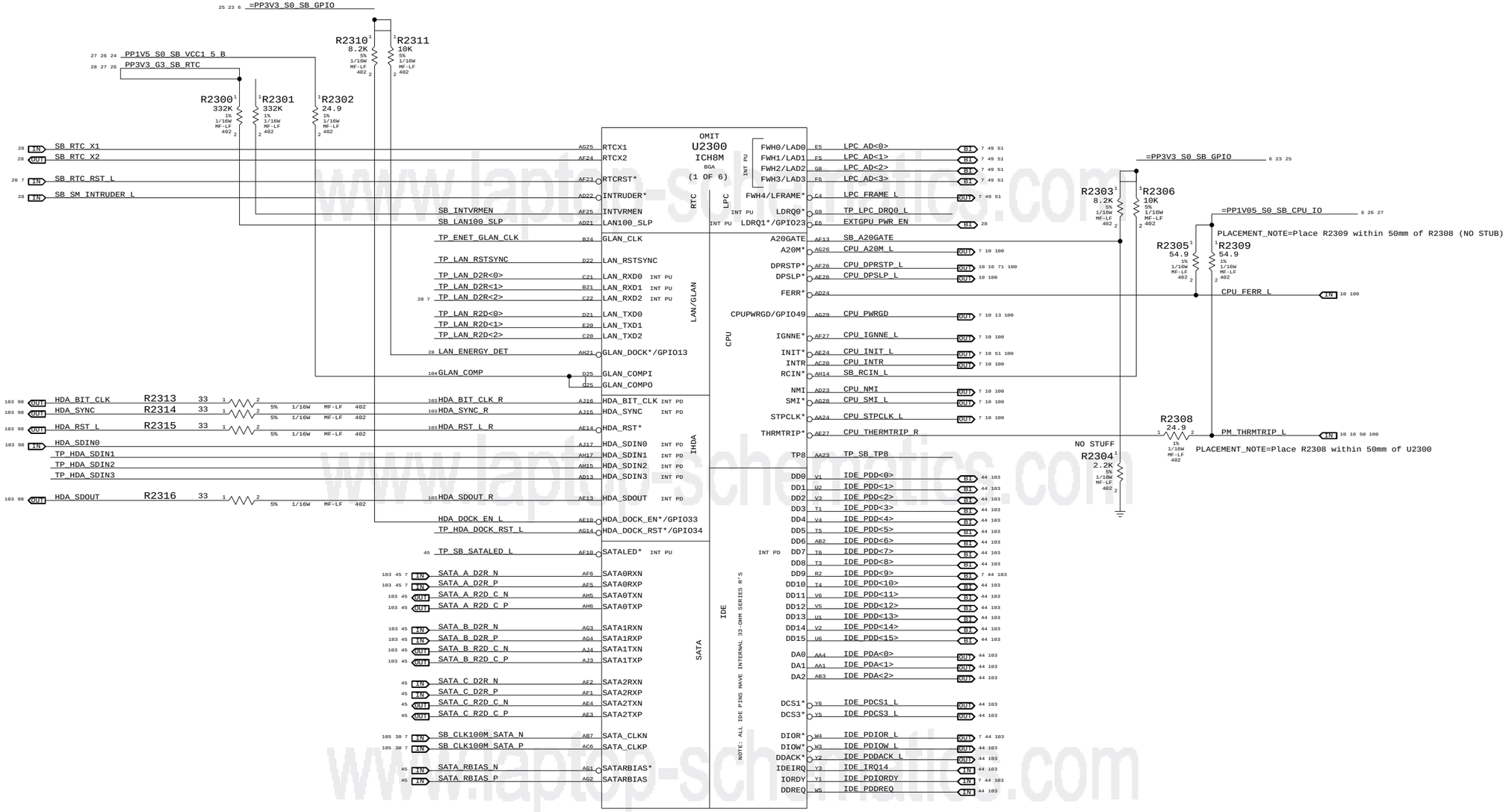
PP0V9_S3M_MEM_NBVREFB — =PP0V9_S3M_MEM_NBVREFB 7 16
VOLTAGE=0.9V TRUE
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.25MM

NB Graphics Decoupling

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 22 OF 118	



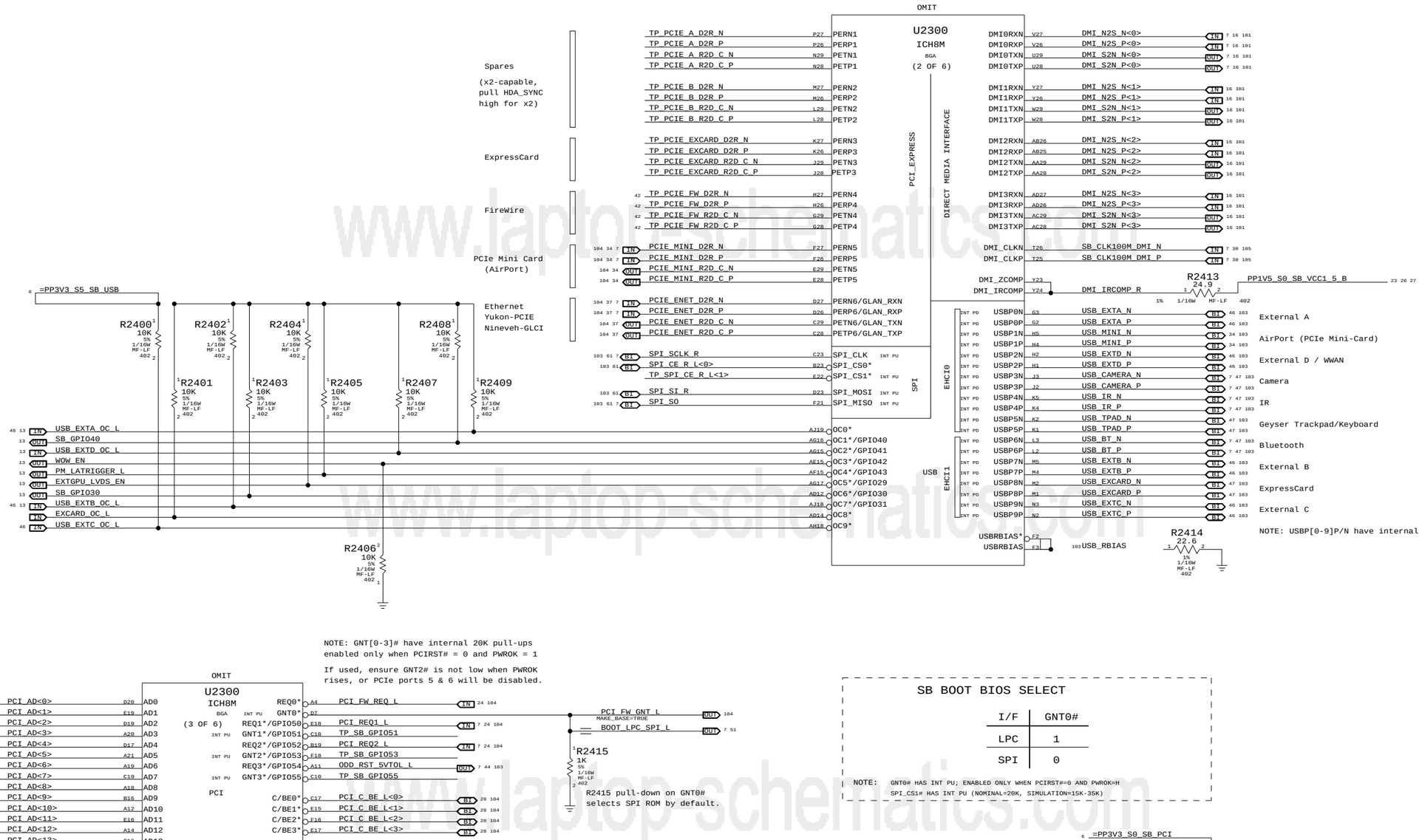
	HDA
HDA_BIT_CLK	24.000MHZ CLOCK W/INTERNAL WEAK PD
HDA_RST#	
HDA_SDIN[0-2]	INTEGRATED PDs
HDA_SDOUT	INTEGRATED PD
ACZ_SYNC	INTEGRATED PD

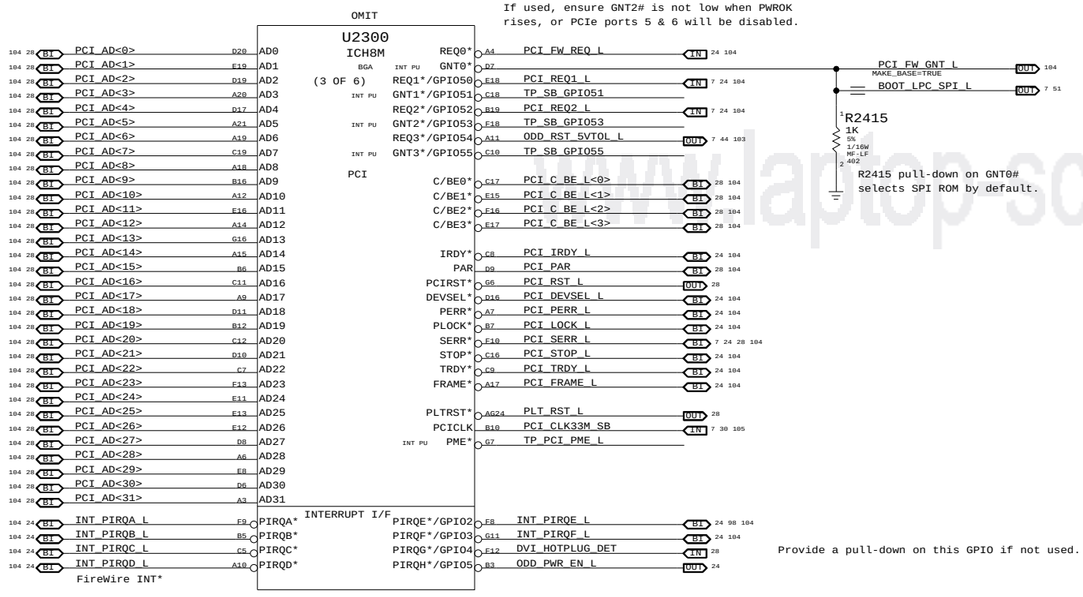
SB Enet, Disk, FSB, LPC

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=06/08/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 23 OF 118	





SB BOOT BIOS SELECT

I/F	GNT0#
LPC	1
SPI	0

NOTE: GNT0# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
SPI_CS1# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)

=PP3V3_S0_SB_PCI

PCI_FRAME_L	R2423	8.2K
PCI_IRDY_L	R2424	8.2K
PCI_TRDY_L	R2425	8.2K
PCI_STOP_L	R2426	8.2K
PCI_SERR_L	R2427	8.2K
PCI_DEVSEL_L	R2428	8.2K
PCI_PERR_L	R2430	8.2K
PCI_LOCK_L	R2429	8.2K
PCI_FW_REQ_L	R2432	8.2K
PCI_REQ1_L	R2431	8.2K
PCI_REQ2_L	R2433	8.2K
INT_PIRQA_L	R2437	8.2K
INT_PIRQB_L	R2436	8.2K
INT_PIRQC_L	R2438	8.2K
INT_PIRQD_L	R2439	8.2K
INT_PIRQE_L	R2440	8.2K
INT_PIRQF_L	R2441	8.2K
ODD_PWR_EN_L	R2442	8.2K

SB PCI, PCIe, DMI, USB

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=06/08/2007

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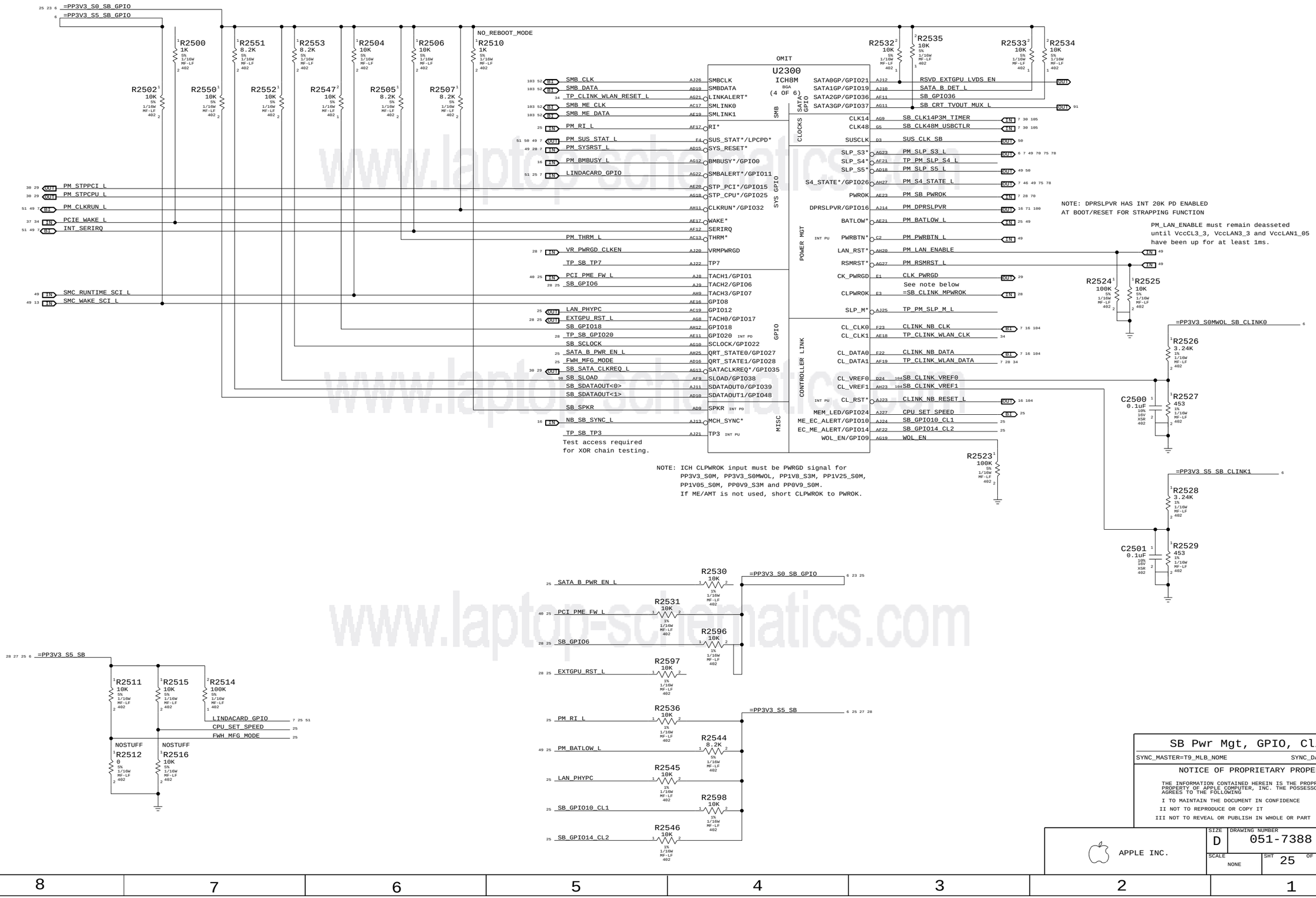
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 24 OF 118	



SB Pwr Mgt, GPIO, Clink	
SYNC_MASTER=T9_MLB_NOME	SYNC_DATE=06/08/2007

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APPLE INC.	SIZE D	DRAWING NUMBER 051-7388	REV. A
	SCALE NONE	SHT 25 OF 118	

U2300
ICH8M
BGA
(5 OF 6)
OMIT

VSS
VSS
VSS_NCTF

6 uA S0-G3
1 mA
1 mA S0-S5
657 mA
47 mA
1080 mA (VCC1_5_A total)
10 mA
19 mA S0, 63 mA M1 & WOL
23 mA
80 mA
1 mA

28 27 23 PP3V3_G3_SB_RTC → VCCRTC
27 PP5V_S0_SB_V5REF → V5REF
27 PP5V_S5_SB_V5REF_SUS → V5REF_SUS
27 24 23 PP1V5_S0_SB_VCC1_5_B → VCC1_5_B
27 PP1V5_S0_SB_VCCSATAPLL → VCCSATAPLL
27 6 =PP1V5_S0_SB_VCC1_5_A_ARX → VCC1_5_A (ARX)
27 6 =PP1V5_S0_SB_VCC1_5_A_ATX → VCC1_5_A (ATX)
6 =PP1V5_S0_SB_VCC1_5_A → VCC1_5_A
27 6 =PP1V5_S0_SB_VCC1_5_A_USB_CORE → VCC1_5_A (USB CORE)
27 6 =PP1V5_S0_SB_VCCUSBPLL → VCCUSBPLL
TP_VCCLAN1_05_INTERNAL_REG1
TP_VCCLAN1_05_INTERNAL_REG2 → VCCLAN1_05
27 6 =PP3V3_S0MWOL_SB_VCCCL3_3 → VCCCL3_3
27 PP1V5_S0_SB_VCCGLANPLL → VCCGLANPLL
27 =PP1V5_S0_SB_VCCGLAN1_5 → VCCGLAN1_5 (GLAN POWER)
6 =PP3V3_S0_SB_VCCGLAN3_3 → VCCGLAN3_3

U2300
ICH8M
BGA
(6 OF 6)
OMIT

VCCA3GP
VCC1_5_A24

CORE
VCC1_05 =PPVCORE_S0_SB (6 27) 1130 mA

VCCDMIPLL R29 PP1V5_S0_SB_VCCDMIPLL (27) 23 mA

VCC_DMI AE28 =PP1V25_S0_SB_DMI (6 27) 50 mA
VCC_DMI AE29

V_CPU_IO AC23 =PP1V05_S0_SB_CPU_IO (6 23 27) 1 mA
V_CPU_IO AC24

VCC3_3 AE29 =PP3V3_S0_SB_VCC3_3_DMI (6 27)
VCC3_3 AD2 =PP3V3_S0_SB_VCC3_3_SATA (6 27)

VCCP CORE
VCC3_3 AC8 AD8 AE8 AF8 =PP3V3_S0_SB_VCC3_3_VCCPCORE (6)

IDE
VCC3_3 AA3 U7 V7 W1 W6 W7 Y7 =PP3V3_S0_SB_VCC3_3_IDE (6 27) 442 mA

PCI
VCC3_3 A8 B15 B18 B4 B9 C15 D13 D5 E10 E7 F11 =PP3V3_S0_SB_VCC3_3_PCI (6 27)

(VCC3_3 total)

VCCHDA AC12 =PP3V3R1V5_S0_SB_VCCHDA (6 27) 32 mA
VCCSUSHDA AD11 =PP3V3_S5_SB_3V3_VCCSUSHDA (6 27) 11 mA S0, 1 mA S3-S5

VCCSUS1_05 J6 TP_VCCSUS1_05_INTERNAL_REG1
VCCSUS1_05 AE20 TP_VCCSUS1_05_INTERNAL_REG2
VCCSUS1_5 AC16 TP_VCCSUS1_5_INTERNAL_REG1
VCCSUS1_5 J7 TP_VCCSUS1_5_INTERNAL_REG2
VCCSUS3_3 C3 =PP3V3_S5_SB_VCCSUS3_3 (6 27)

VCCP SUS
VCCSUS3_3 AC18 AC21 AC22 AG20 AH28

VCCP PUSB
VCCSUS3_3 P6 P7 C1 N7 P1 P2 P3 P4 P5 R1 R3 R5 R6 =PP3V3_S5_SB_VCCSUS3_3_USB (6 27)

(VCCSUS3_3 total) 117 mA S0, 44 mA S3-S5

VCCCL1_05 G22 TP_VCCCL1_05_INTERNAL_REG
VCCCL1_5 A22 VCCCL1_5V

VCCLAN3_3 F19 =PP3V3_S0MWOL_SB_VCCLAN3_3 (6 27) 19 mA S0, 51 mA M1 & WOL

C2600 1uF 10% 6.3V CERM 402
C2601 0.1uF 20% 10V CERM 402

NOTE:
VccHDA and VccSusHDA can be 1.5V or 3.3V depending on VIO of HD Audio interface.

Current figures provided assume 1.5V.

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

SB Power & Ground

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=06/08/2007

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 26 OF 118	

=PP3V3_S5_SB
=PP5V_S5_SB
1 mA S0-S5

ICH V5REF_SUS Filter & Follower
(ICH Reference for 5V Tolerance on Resume Well Inputs)

R2701 10 5% 1/16W MF-LF 402
CRITICAL
D2702 BAT54DW SOT-363
PP5V_S5_SB_V5REF_SUS
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2704 0.1UF 10% 16V X5R 402
1 mA S0-S5

PLACEMENT NOTE:
PLACE C2704 < 2.54MM OF PIN G4 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

=PP3V3_S0_SB
=PP5V_S0_SB
1 mA

ICH V5REF Filter & Follower
(ICH Reference for 5V Tolerance on Core Well Inputs)

R2702 100 5% 1/16W MF-LF 402
CRITICAL
D2702 BAT54DW SOT-363
PP5V_S0_SB_V5REF
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=5V
C2703 1UF 10% 16V X5R 402-1
1 mA

PLACEMENT NOTE:
PLACE C2703 < 2.54MM OF PIN A16..T7 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY

PLACEMENT NOTE:
PLACE C2700 & C2705-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
DISTRIBUTED BETWEEN AA25..V23

=PP1V5_S0_SB
837 mA
CRITICAL
L2700 FERR-330-OHM-1.5A 0805-1
CRITICAL
C2700 220UF 20% 16V ELEC SM-CASE-C1
C2705 22UF 20% 6.3V CERM 805
C2706 22UF 20% 6.3V CERM 805
C2707 2.2UF 20% 6.3V CERM1 603

ICH VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.5V
MAKE_BASE=TRUE
657 mA

=PP1V5_S0_SB_VCCGLAN1_5
80 mA
PLACEMENT NOTE:
PLACE C2736 NEAR PIN B27..A26
C2736 4.7uF 20% 6.3V CERM 603

ICH VCCGLANPLL FILTER REMOVED PER SR DG
(ICH GLAN PLL PWR)
PP1V5_S0_SB_VCCGLANPLL
33 mA
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN A24
C2732 2.2uF 20% 6.3V CERM1 603

ICH VCCSATAPLL Filter
(ICH SATA PLL PWR)
R2735 0 5% 1/16W MF-LF 402
PP1V5_S0_SB_VCCSATAPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
47 mA
CRITICAL
L2702 10UH-100MA 0805
C2735 10UF 20% 6.3V X5R 603
C2717 1UF 10% 6.3V CERM 402
PP1V5_S0_SB_VCCSATAPLL
47 mA
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AJ6

ICH VCCDMIPLL Filter
(ICH DMI PLL PWR)
R2700 1 5% 1/10W MF-LF 603
PP1V5_S0_SB_VCCDMIPLL_F
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=1.5V
23 mA
CRITICAL
L2703 1.0UH-0.5A 1210
C2708 10UF 20% 6.3V X5R 603
C2701 0.01UF 10% 16V CERM 402
PP1V5_S0_SB_VCCDMIPLL
23 mA
PLACEMENT NOTE:
PLACE CAPS < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY

Current numbers from ICH8M Max Power Estimates Rev 2.0, doc #610194.

ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
0.6 uA G3
PP3V3_G3_SB_RTC
C2729 0.1UF 10% 16V X5R 402
C2730 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS NEAR PIN AD25 OF SB

ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2731 0.1UF 10% 16V X5R 402
C2734 0.1UF 10% 16V X5R 402
117 mA S0 /
44 mA S3-S5
(VCCSUS3_3 Total)
PLACEMENT NOTE:
PLACE CAPS NEAR PINS AC18..AH28

ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAP NEAR PINS
P6..R6
C2733 4.7uF 20% 6.3V CERM 603

ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
38 mA S0 /
114 mA M1 & WOL
=PP3V3_S0MWOL_SB_VCCLAN3_3
=PP3V3_S0MWOL_SB_VCCCL3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS
F19 AND G20
C2719 0.1UF 10% 16V X5R 402

ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA3...Y7
C2725 0.1UF 10% 16V X5R 402

=PP3V3_S0_SB_VCC3_3_SATA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD2
C2738 0.1UF 10% 16V X5R 402

442 mA
(VCC3_3 Total)
=PP3V3_S0_SB_VCC3_3_DMI
PLACEMENT NOTE:
PLACE CAP < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AF29
C2737 0.1UF 10% 16V X5R 402

ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
C2726 0.1UF 10% 16V X5R 402
C2727 0.1UF 10% 16V X5R 402
C2728 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A8 ... F11

ICH VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V/1.5V PWR)
32 mA
(@ 1.5V)
=PP3V3R1V5_S0_SB_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AC12
C2721 0.1UF 10% 16V X5R 402

ICH VCCSUSHDA BYPASS
(ICH INTEL HDA SUSPEND 3.3V/1.5V PWR)
11 mA S0 /
1 mA S3-S5
(@ 1.5V)
=PP3V3_S5_SB_3V3_VCCSUSHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AD11
C2741 0.1UF 10% 16V X5R 402

ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AE7..AJ7
C2711 1UF 10% 6.3V CERM 402

ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
1080 mA
(VCC1_5_A Total)
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AC1..AC5
C2714 1UF 10% 6.3V CERM 402

ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS F1..M7
C2712 0.1UF 10% 16V X5R 402

ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
10 mA
=PP1V5_S0_SB_VCCUSBPLL
PLACEMENT NOTE:
PLACE C2715 NEAR PIN D1 OF SB
C2715 0.1UF 10% 16V X5R 402

50 mA
=PP1V25_S0_SB_DMI
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY
OR 3.56MM ON PRIMARY NEAR PIN AE29
C2739 22UF 20% 6.3V CERM 805

ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
1130 mA
=PPVCORE_S0_SB
C2718 0.1UF 10% 16V X5R 402
C2702 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB

ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
1 mA
=PP1V05_S0_SB_CPU_IO
C2724 4.7UF 20% 6.3V CERM 603
C2723 0.1UF 10% 16V X5R 402
C2722 0.1UF 10% 16V X5R 402
PLACEMENT NOTE:
PLACE NEAR PINS AC23,AC24 OF SB

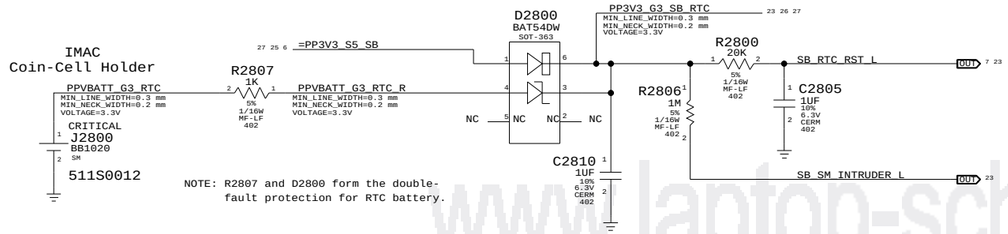
SB Decoupling

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

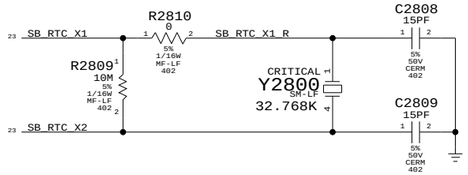
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 27 OF 118	

RTC Power Sources



SB RTC Crystal



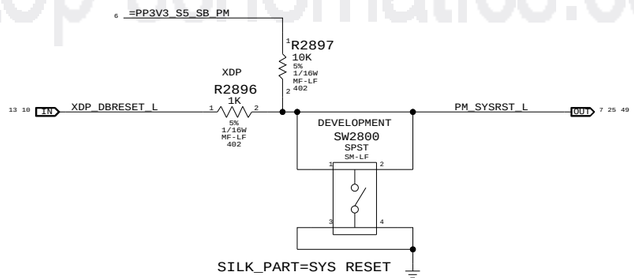
CPU VCORE FORCEPSI UNUSED

PWROK = CLINK PWROK FOR NO ME

VRMPWRGD INVERTER

UNUSED PCI BUS

PCI_AD<0>	MAKE_BASE=TRUE	TP_PCI_AD_0	
PCI_AD<1>	MAKE_BASE=TRUE	TP_PCI_AD_1	
PCI_AD<2>	MAKE_BASE=TRUE	TP_PCI_AD_2	
PCI_AD<3>	MAKE_BASE=TRUE	TP_PCI_AD_3	
PCI_AD<4>	MAKE_BASE=TRUE	TP_PCI_AD_4	NO_TEST=TRUE
PCI_AD<5>	MAKE_BASE=TRUE	TP_PCI_AD_5	
PCI_AD<6>	MAKE_BASE=TRUE	TP_PCI_AD_6	
PCI_AD<7>	MAKE_BASE=TRUE	TP_PCI_AD_7	
PCI_AD<8>	MAKE_BASE=TRUE	TP_PCI_AD_8	
PCI_AD<9>	MAKE_BASE=TRUE	TP_PCI_AD_9	
PCI_AD<10>	MAKE_BASE=TRUE	TP_PCI_AD_10	
PCI_AD<11>	MAKE_BASE=TRUE	TP_PCI_AD_11	
PCI_AD<12>	MAKE_BASE=TRUE	TP_PCI_AD_12	
PCI_AD<13>	MAKE_BASE=TRUE	TP_PCI_AD_13	
PCI_AD<14>	MAKE_BASE=TRUE	TP_PCI_AD_14	
PCI_AD<15>	MAKE_BASE=TRUE	TP_PCI_AD_15	
PCI_AD<16>	MAKE_BASE=TRUE	TP_PCI_AD_16	
PCI_AD<17>	MAKE_BASE=TRUE	TP_PCI_AD_17	
PCI_AD<18>	MAKE_BASE=TRUE	TP_PCI_AD_18	
PCI_AD<19>	MAKE_BASE=TRUE	TP_PCI_AD_19	
PCI_AD<20>	MAKE_BASE=TRUE	TP_PCI_AD_20	
PCI_AD<21>	MAKE_BASE=TRUE	TP_PCI_AD_21	
PCI_AD<22>	MAKE_BASE=TRUE	TP_PCI_AD_22	
PCI_AD<23>	MAKE_BASE=TRUE	TP_PCI_AD_23	
PCI_AD<24>	MAKE_BASE=TRUE	TP_PCI_AD_24	
PCI_AD<25>	MAKE_BASE=TRUE	TP_PCI_AD_25	
PCI_AD<26>	MAKE_BASE=TRUE	TP_PCI_AD_26	
PCI_AD<27>	MAKE_BASE=TRUE	TP_PCI_AD_27	
PCI_AD<28>	MAKE_BASE=TRUE	TP_PCI_AD_28	
PCI_AD<29>	MAKE_BASE=TRUE	TP_PCI_AD_29	
PCI_AD<30>	MAKE_BASE=TRUE	TP_PCI_AD_30	
PCI_AD<31>	MAKE_BASE=TRUE	TP_PCI_AD_31	
PCI_C_BE_L<0>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_0	
PCI_C_BE_L<1>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_1	
PCI_C_BE_L<2>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_2	
PCI_C_BE_L<3>	MAKE_BASE=TRUE	TP_PCI_C_BE_L_3	
PCI_RST_L	MAKE_BASE=TRUE	TP_PCI_RST_L	
PCI_PAR	MAKE_BASE=TRUE	TP_PCI_PAR	

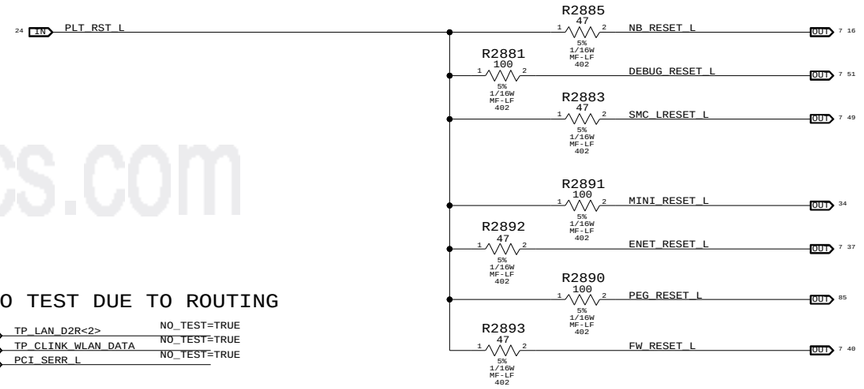


NO TEST DUE TO ROUTING

TP_LAN_D2R<2>		NO_TEST=TRUE
TP_CLINK_WLAN_DATA		NO_TEST=TRUE
PCI_SERR_L		NO_TEST=TRUE

Platform Reset Connections

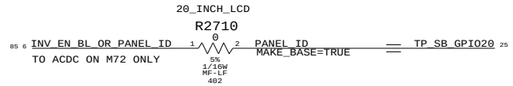
Unbuffered



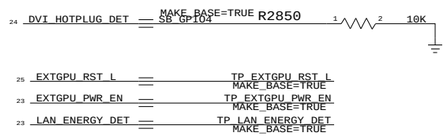
RE-PURPOSED GPIOS

SB_GPIO6	MAKE_BASE=TRUE	GPU_PRESENT

20_INCH_LCD



UNUSED GPIOS



SB Misc

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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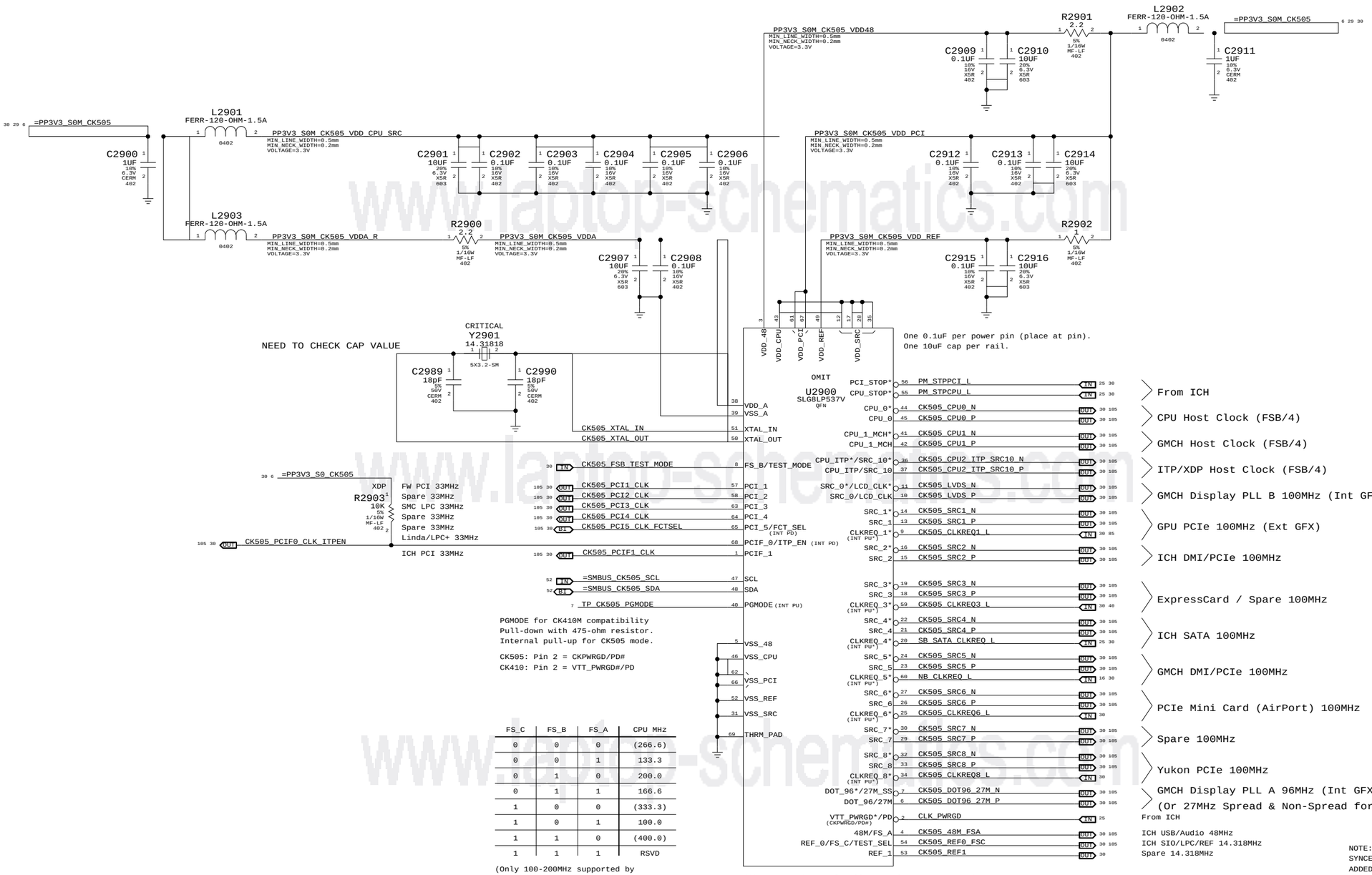
SCALE: NONE	SHT 28 OF 118	



FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

(Only 100-200MHz supported by SLG8LP536 and CY28545-5)

FCT_SEL	PIN 6	PIN 7	PIN 10	PIN 11	
0	DOT_96+	DOT_96-	LCD_CLK+	LCD_CLK-	(For Internal Graphics)
1	27M	27M w/SS	SRC_0+	SRC_0-	(For External Graphics)

NOTE:
SYNCED FROM T9_MLB_NOME
ADDED 475-OHM RESISTOR TO NB_CLKREQ_L PER INTEL
DELETED RES AFTER INTEL SAID IT'S NOT NEEDED!

Clock (CK505)

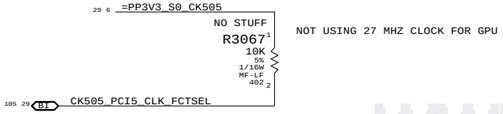
SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

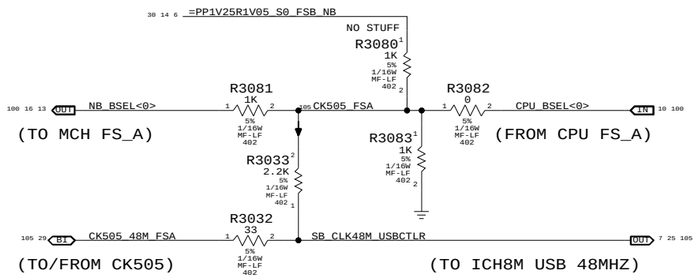
SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 29 OF 118	

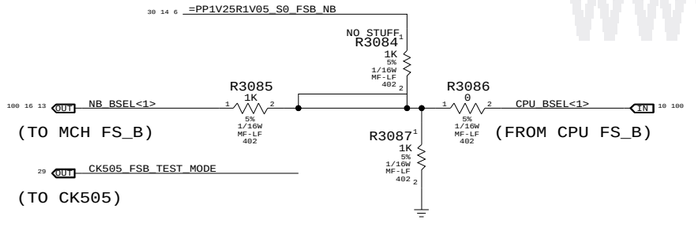
CK505 Configuration Straps

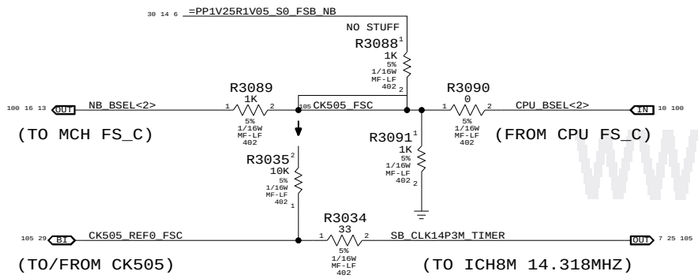
FCT_SEL (GFX clock select)



FS_A, FS_B, FS_C (Host clock freq select)





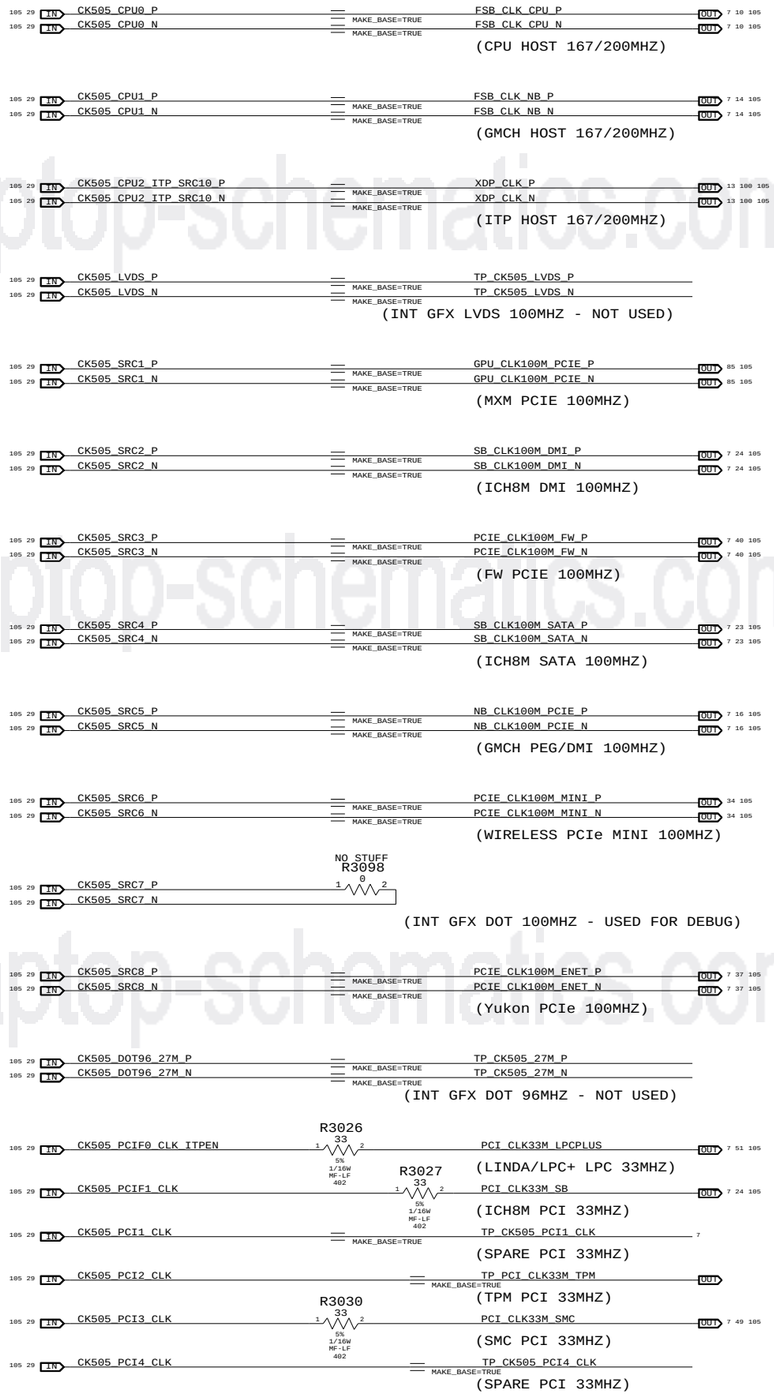


FS_C	FS_B	FS_A	CPU MHz
0	0	0	(266.6)
0	0	1	133.3
0	1	0	200.0
0	1	1	166.6
1	0	0	(333.3)
1	0	1	100.0
1	1	0	(400.0)
1	1	1	RSVD

NO STUFF R3082, R3086 & R3090
for manual CPU clk frequency.

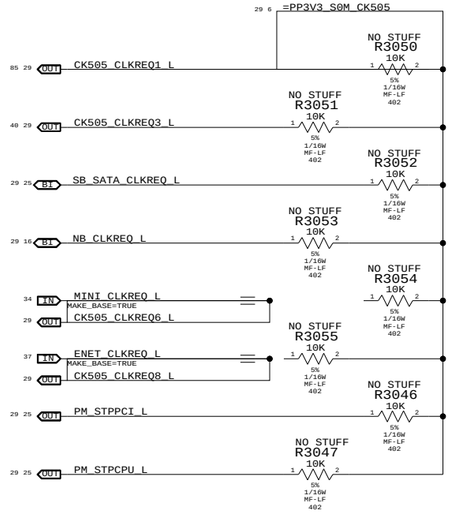
CLK Termination

(Note: HOST/SRC/GFX clock termination kept on T9 for Cypress CY28545-5 compatibility)



CLKREQ Controls

Silego SL8GLP537 has internal
PULL-UPS ON ALL CLKREQ# PINS?



Unused Clocks

Clock Termination

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 30 OF 118	

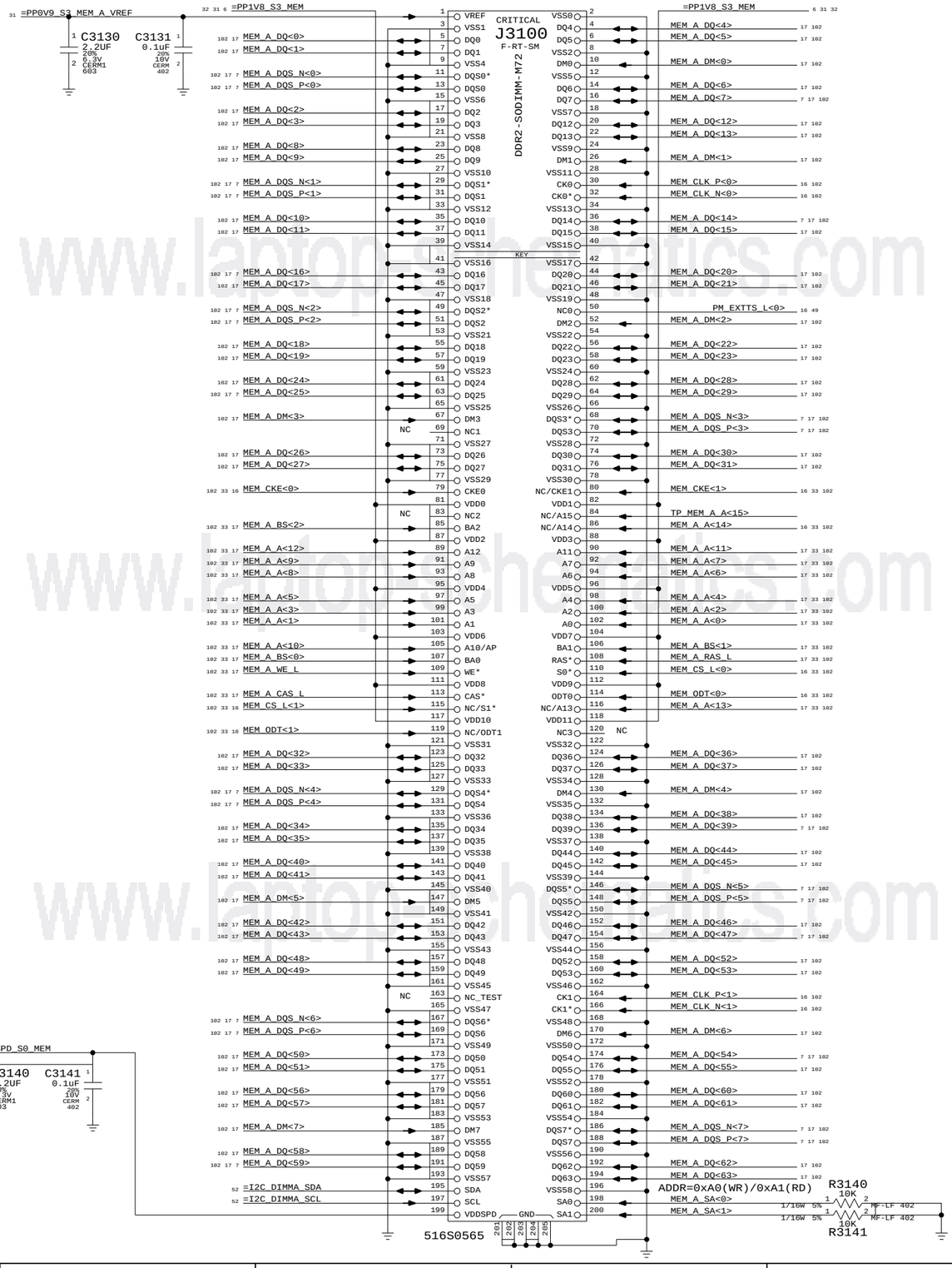
Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

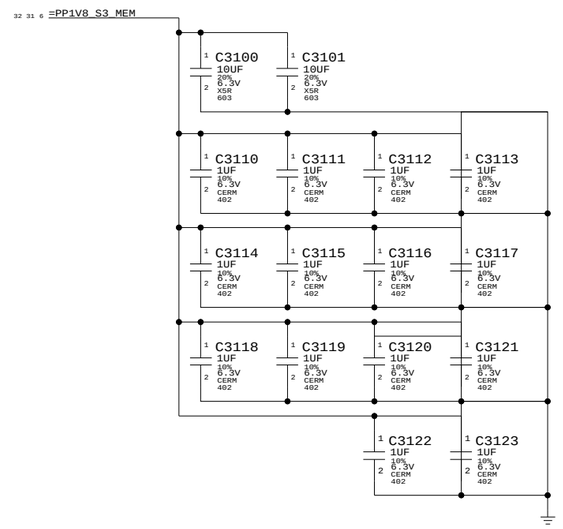
BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.



DDR2 Bypass Caps

(For return current)



DDR2 SO-DIMM Connector A

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE SHT 31 OF 118

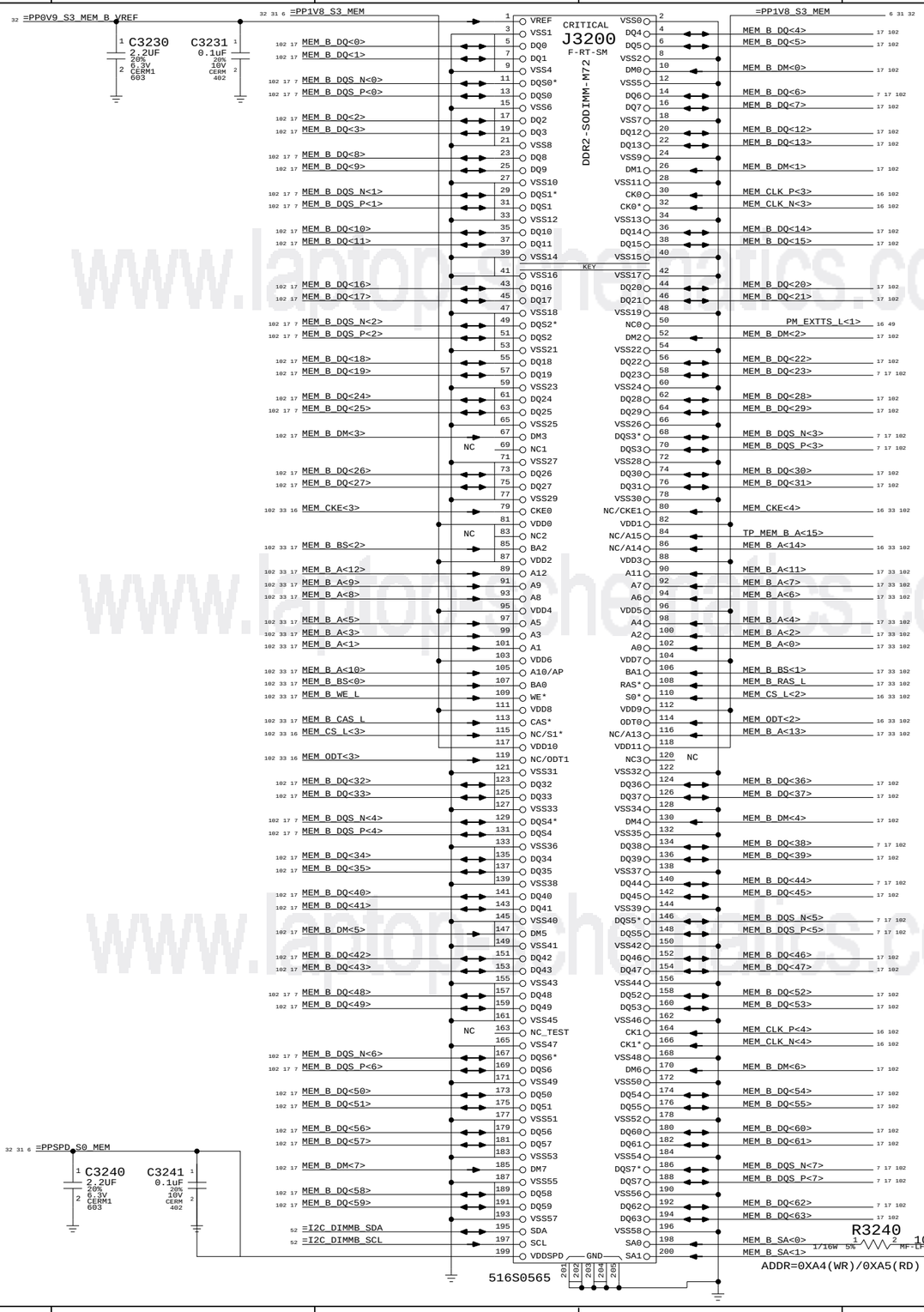
Page Notes

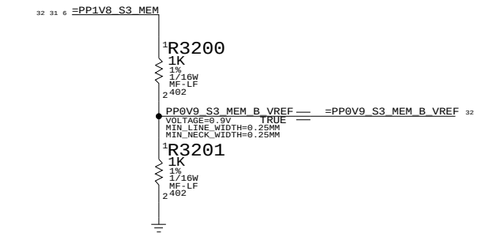
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PP0V9_S3_MEM_VREF
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_MEM_SCL
- =I2C_MEM_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF.
The reference voltage must be provided
by another page.





DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector B

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

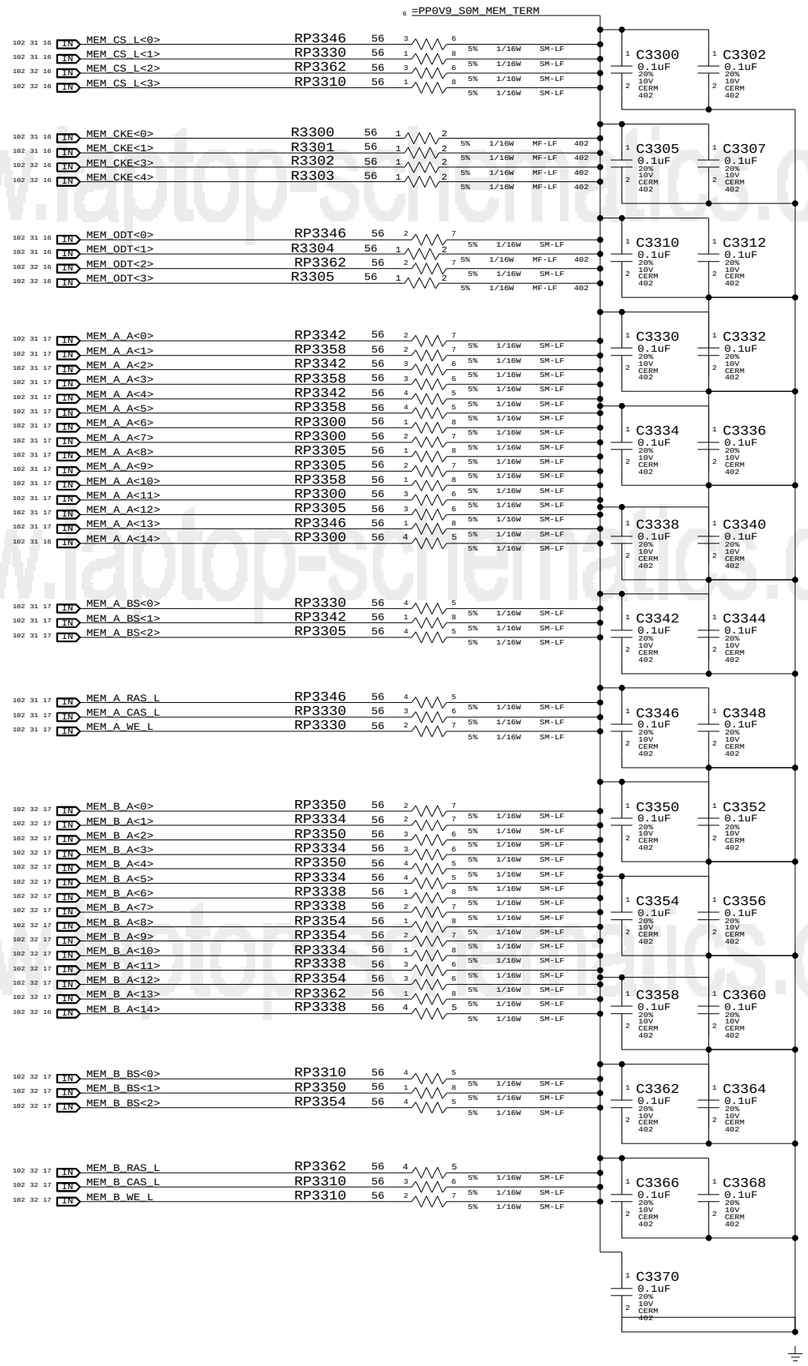
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE SHT 32 OF 118

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE

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	3.3V_S3_CURRENT	D0-D2_D3HOT	D3COLD
MAX CONT:		1100MA	250MA
MAX PEAK		2750MA	2750MA
1.5V_CURRENT			
MAX CONT:		375MA	N/A
MAX PEAK		560MA	N/A

NOTE: CURRENT DATA PER 5/16/2005 PCIE MINI CEM ECN

NO STUFF
R3400
0
5%
1/16W
MF-LF
402

NO STUFF
R3401
0
5%
1/16W
MF-LF
402

CRITICAL
J3400
ASOB226-S80N-7F
F-RT-SM

=PP3V3_S3_MINI 6

C3410 0.1uF 20% 10V CERM 402
C3420 0.1uF 20% 10V CERM 402
C3421 10uF 20% 6.3V X5R 603

PP1V05_S0 6 7 73

=PP1V5_S0_MINI 6

C3400 0.1uF 20% 10V CERM 402
C3401 10uF 20% 6.3V X5R 603

37 25 OUT PCIE_WAKE_L
RSVD_MINI_WLAN_ACTIVE
RSVD_MINI_BT_ACTIVE
30 OUT MINI_CLKREQ_L
105 30 IN PCIE_CLK100M_MINI_N
105 30 IN PCIE_CLK100M_MINI_P
RESERVED
RESERVED

104 24 7 OUT PCIE_MINI_D2R_N
104 24 7 OUT PCIE_MINI_D2R_P

PLACEMENT_NOTE=Place close to U2300.
C3431
0.1uF
10%
16V
X5R
402

104 24 IN PCIE_MINI_R2D_C_N

PLACEMENT_NOTE=Place close to U2300.
C3430
0.1uF
10%
16V
X5R
402

104 24 IN PCIE_MINI_R2D_C_P

104 PCIE_MINI_R2D_N
104 PCIE_MINI_R2D_P

MINI_RESET_L IN 28

=SMBUS_MINI_SCL IN 52
=SMBUS_MINI_SDA BI 52

USB_MINI_N BI 24 103
USB_MINI_P BI 24 103

NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC
NC

516S0391

CLINK_WLAN_CLK = TP_CLINK_WLAN_CLK 25
MAKE_BASE=TRUE

CLINK_WLAN_DATA = TP_CLINK_WLAN_DATA 7 25 28
MAKE_BASE=TRUE

CLINK_WLAN_RESET_L = TP_CLINK_WLAN_RESET_L 25
MAKE_BASE=TRUE

STANDOFF FOR J3400
CRITICAL
SDF3400
STDOFF-4OD5.6H-1.35-TH
SDF3400_1
860-0691

R3410
0
5%
1/16W
MF-LF
402

PCI-E MiniCard Connector

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 34 OF 118	

Page Notes

Power aliases required by this page:
- =PP3V3_ENET_PHY (EC / Ultra)
- =PP1V9R2V5_ENET_PHY (2.5V / 1.8V)

- =PP1V2_ENET_PHY

Signal aliases required by this page:
- =ENET_CLKREQ_L (NC/TP for Yukon EC)
- =ENET_VMAIN_AVLBL (See note by pin)

38 =PP1V2_ENET_PHY
Yukon Ultra
No link: 130 mA
10 Mbps: 130 mA
100 Mbps: 150 mA
1000 Mbps: 290 mA
NOSTUFF C3700 4.7UF 20% 6.3V CERM 603
C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 1UF 10% 10V X5R 402

38 =PP3V3_ENET_PHY
Yukon Ultra
No link: 60 mA
10 Mbps: 70 mA
100 Mbps: 70 mA
1000 Mbps: 80 mA
NOSTUFF C3710 4.7UF 20% 6.3V CERM 603
C3711 C3712 C3713 C3714 C3715 1UF 10% 10V X5R 402

39 38 PP1V9_S3_ENET
R3720 0 5% 1/10W MF-LF 402
104 PP1V9_ENET_PHY_AVDD
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.8V
Yukon Ultra (1.8V)
No link: 0 mA
10 Mbps: 30 mA
100 Mbps: 40 mA
1000 Mbps: 150 mA
C3720 4.7UF 20% 6.3V CERM 603
C3721 C3722 C3723 C3724 1UF 10% 10V X5R 402

104 24 7 OUT PCIE_ENET_D2R_P
104 24 7 OUT PCIE_ENET_D2R_N
C3735 0.1uF 10% 16V X5R 402
C3736 0.1uF 10% 16V X5R 402
104 24 IN PCIE_ENET_R2D_C_P
104 24 IN PCIE_ENET_R2D_C_N
C3730 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3730 close to southbridge.
C3731 0.1uF 10% 16V X5R 402
PLACEMENT_NOTE=Place C3731 close to southbridge.
105 30 7 IN PCIE_CLK100M_ENET_P
105 30 7 IN PCIE_CLK100M_ENET_N
30 OUT ENET_CLKREQ_L
34 25 OUT PCIE_WAKE_L
28 7 IN ENET_RESET_L
104 39 BI ENET_MDI_P<0>
104 39 BI ENET_MDI_N<0>
104 39 BI ENET_MDI_P<1>
104 39 BI ENET_MDI_N<1>
104 39 BI ENET_MDI_P<2>
104 39 BI ENET_MDI_N<2>
104 39 BI ENET_MDI_P<3>
104 39 BI ENET_MDI_N<3>
R3740 R3741 R3742 R3743 R3744 R3745 R3746 R3747 49.9 1% 1/16W MF-LF 402
ENET_MDI0 ENET_MDI1 ENET_MDI2 ENET_MDI3
C3740 C3742 C3744 C3746 0.001UF 10% 50V CERM 402
CRITICAL Y3750 25.0000M SM-3-LF 197S0167 CL = 20PF
C3750 C3751 27PF 5% 50V CERM 402
7 ENET_CLK25M_XTALI
7 ENET_CLK25M_XTALO

U3700 88E8058 QFN
CRITICAL
NC_32 NC_51 NC_52 NC_57 NC_64 AVDD0 AVDD1 AVDD2 AVDD3 VDDO_TTL0 VDDO_TTL1 VDDO_TTL2 VDDO_TTL3 AVDDH VDD0 VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7
PCI EXPRESS
108 PCIE_ENET_D2R_C_P TX_P
108 PCIE_ENET_D2R_C_N TX_N
108 7 PCIE_ENET_R2D_P RX_P
108 7 PCIE_ENET_R2D_N RX_N
55 REFCLKP
56 REFCLKN
42 CLKREQ*
6 WAKE*
5 PERST*
ANALOG
17 MDIP0
18 MDIN0
20 MDIP1
21 MDIN1
26 MDIP2
27 MDIN2
30 MDIP3
31 MDIN3
MEDIA
15 XTALI
14 XTALO
MAIN CLK
65 THRML_PAD
LOM_DISABLE* 10 ENET_LOM_DIS_L
VAUX_AVLBL 12
SWITCH_VAUX 9 NC
VMAIN_AVLBL 47 Must be high in S0 state (can use PP3V3_S0 as input) =ENET_VMAIN_AVLBL IN 38
SWITCH_VCC 11 NC
CTRL18 4 TP_YUKON_CTRL18 OUT 38
CTRL12 3 TP_YUKON_CTRL12 OUT 38
RSET 16 YUKON_RSET
R3760 4.7K 5% 1/16W MF-LF 402
R3765 4.99K 1% 1/16W MF-LF 402
LED
LED_ACT* 59 ENET_LED_ACT_L 39
LED_LINK10/100* 60 ENET_LED_LINK10_100_L 39
LED_LINK1000* 62 ENET_LED_LINK1000_L 39
LED_DUPLEX* 63 ENET_LED_LINK_L 39
SPI
(IPU) SPI_DO 34 NC
(IPU) SPI_DI 35 NC
(IPU) SPI_CLK 37 NC
(IPU) SPI_CS 36 NC
TWSI
(IPU) VPD_CLK 38 YUKON_VPD_CLK
(IPU) VPD_DATA 41 YUKON_VPD_DATA
TEST/RSVD
(IPD) TESTMODE 46
RSVD_24 24 NC
RSVD_25 25 NC
RSVD_29 29 NC
RSVD_43 43 NC

VPD ROM
C3780 0.1UF 10% 16V X5R 402
R3780 4.7K 5% 1/16W MF-LF 402
R3781 4.7K 5% 1/16W MF-LF 402
U3780 M24C08 SO8
E2 NC1 NC0 WC* VCC OMIT SDA SCL VSS
NC NC
CRITICAL

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S2060	1	IC,FLASH,88E8058 ETHERNET VPD,IIC,SO8	U3780	CRITICAL	

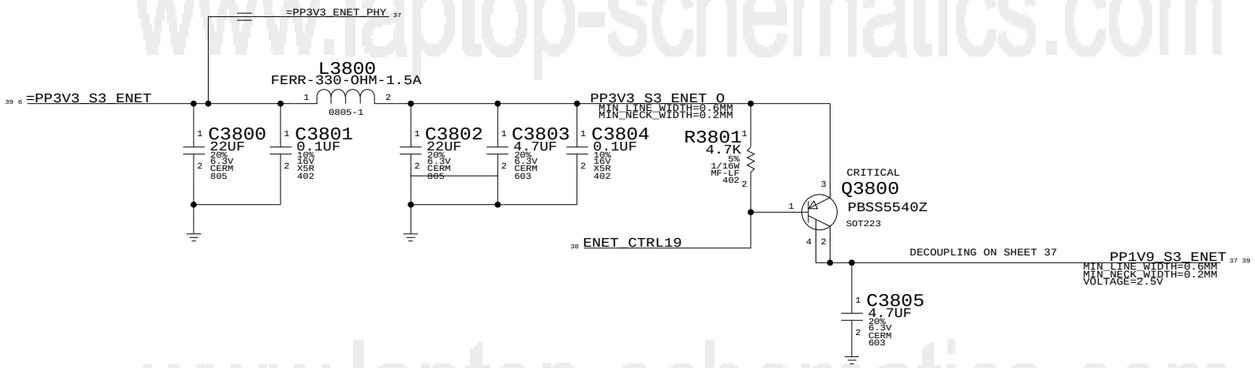
Ethernet (Yukon)

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

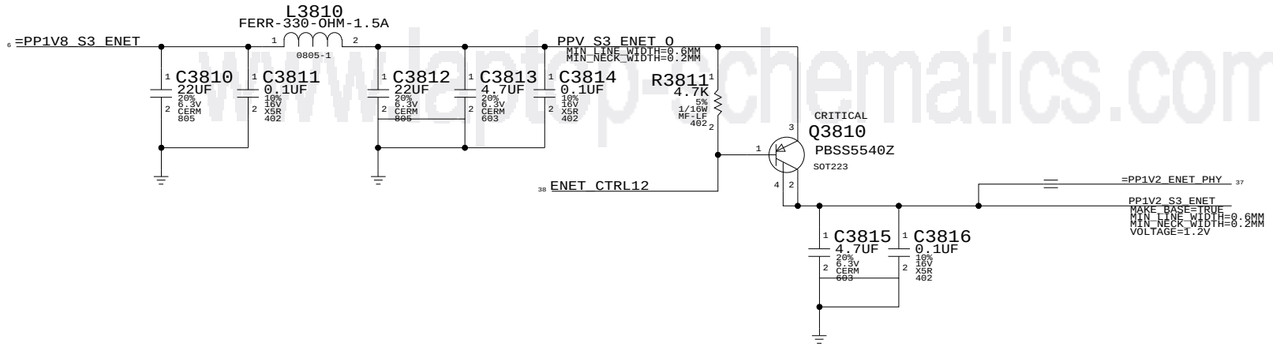
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 37 OF 118	

YUKON 1.9V SUPPLY



YUKON 1.2 RAIL SUPPLY



YUKON T9 ALIASES

37 TP_YUKON_CTRL18	=	ENET_CTRL19 MAKE_BASE=TRUE	38
37 TP_YUKON_CTRL12	=	ENET_CTRL12 MAKE_BASE=TRUE	38
37 =ENET_VMAIN_AVLBL	=	=PP3V3_S0_ENET	6

YUKON/ULTRA SUPPORT

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 38 OF 118	

38 37 PP1V9_S3_ENET

R3900
0
5%
1/10W
MF-LF
402

PP1V9_ENET_CTAP
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm
VOLTAGE=1.9V

C3900 0.1UF 20% 10V CERM 402
C3901 0.001UF 10% 50V CERM 402
C3902 0.001UF 10% 50V CERM 402
C3903 0.001UF 10% 50V CERM 402

CRITICAL

T3900
LFE9245A-AP
SOI

NOTE: N AND P SWAPPED FOR ROUTING!!!

104 37 ENET_MDI_N<0>	14 MX4+	1CT:1CT	TD4+ 11	108	ENET_MDI_T_N<0>
	15 MCT4		TCT4 10		
104 37 ENET_MDI_P<0>	13 MX4-		TD4- 12	108	ENET_MDI_T_P<0>
104 37 ENET_MDI_N<1>	17 MX3+	1CT:1CT	TD3+ 8	108	ENET_MDI_T_N<1>
	18 MCT3		TCT3 7		
104 37 ENET_MDI_P<1>	16 MX3-		TD3- 9	108	ENET_MDI_T_P<1>
104 37 ENET_MDI_N<2>	20 MX2+	1CT:1CT	TD2+ 5	108	ENET_MDI_T_N<2>
	21 MCT2		TCT2 4		
104 37 ENET_MDI_P<2>	19 MX2-		TD2- 6	108	ENET_MDI_T_P<2>
104 37 ENET_MDI_N<3>	23 MX1+	1CT:1CT	TD1+ 2	108	ENET_MDI_T_N<3>
	24 MCT1		TCT1 1		
104 37 ENET_MDI_P<3>	22 MX1-		TD1- 3	108	ENET_MDI_T_P<3>

SYM (2 OF 2)

NOTE: N AND P SWAPPED BACK FOR HUB COMPATABILITY!!!

(514-0401)
J3900
RJ45-M72
F-ANG-TH

GND_CHASSIS_ENET 9 39

ENET_CTAP <0>
ENET_CTAP <1>
ENET_CTAP <2>
ENET_CTAP <3>

R3910 R3911 R3912 R3913
75
5%
1/16W
MF-LF
402

11/2007 - THIS CAP IS NOW NOSTUFF FOR EMC
SINCE WE HAVE A COMMON GROUND, THIS WAS CAUSING
NOISE ON THE NETWORK CABLE
NOSTUFF
C3910
0.001UF
20%
2KV
CERM
1808

ENET_CTAP_COMMON — GND_CHASSIS_ENET 9 39

NOTE: PLACE CLOSE TO CONNECTOR

38 6 =PP3V3_S3_ENET

DEVELOPMENT
R3901 330
R3902 330
R3903 330
R3904 330
5%
1/10W
MF-LF
603

LED4300_1
LED4301_1
LED4302_1
LED4303_1

DEVELOPMENT
LED3900
LED3901
LED3902
LED3903
GREEN-1.0MCD
2.0X1.25MM-SM

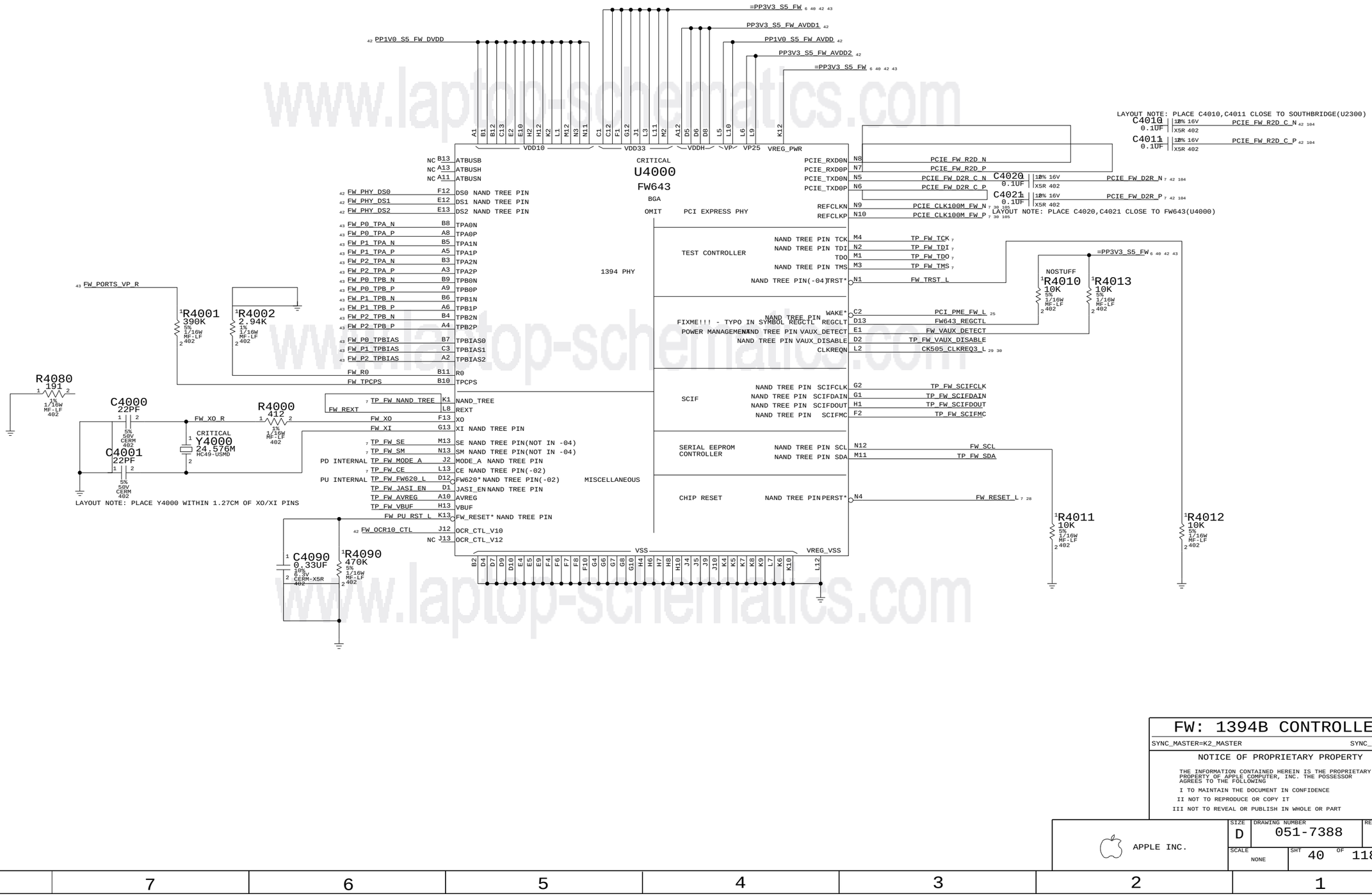
37 ENET_LED_ACT_L
MAKE_BASE=TRUE
37 ENET_LED_LINK10_100_L
MAKE_BASE=TRUE
37 ENET_LED_LINK1000_L
MAKE_BASE=TRUE
37 ENET_LED_LINK_L
MAKE_BASE=TRUE

ETHERNET CONNECTOR

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 39 OF 118	



FW: 1394B CONTROLLER

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

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APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 40 OF 118	

FW643 1.0V GENERATION

USING THE SAME TRICK FOR FW AS FOR ETHERNET. DERIVED FROM MARVELL SCHEMATICS

RF CHOKE TO KEEP DIGITAL NOISE OFF ANALOG SUPPLY RAIL

L4200
120-OHM-0.3A-EMI
0402-LF

PP1V0_S5_FW_AVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.0V
25MA PCIE SERDES

CRITICAL
Q4200
BCP69
SOT223-4

=PP3V3_S5_FW

C4200 2.2UF 20% 6.3V CERM 402-LF
C4201 2.2UF 20% 6.3V CERM 402-LF

R4200
75
5% 1/10W MF-LF 402
FW_OCR10_CTL
FW_OCR10_CTL_R

PP1V0_S5_FW_DVDD
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=1.0V
110MA DIGITAL CORE

C4210 0.1UF 20% 10V CERM 402
C4211 0.1UF 20% 10V CERM 402
C4212 10UF 20% 6.3V CERM 805-1
C4213 10UF 20% 6.3V CERM 805-1

NOTE: MULTIPLE VIAS TO GND
NOTE: Q4200 COLLECTOR CONNECT TO CAPS WITH 0.4 SQ-IN HEAT SINK

1394 PHY DATA/STROBE OPTIONS

=PP3V3_S5_FW

NOSTUFF
R4250 10K 5% 1/16W MF-LF 402
R4251 10K 5% 1/16W MF-LF 402
R4252 10K 5% 1/16W MF-LF 402

FW_PHY_DS0
FW_PHY_DS1
FW_PHY_DS2

THERE ARE THREE FIREWIRE PORTS, BUT ONLY TWO ARE USED. THE PULL-UPS ASSERT/ENABLE DATA STROBE ONLY MODE, WHICH IS SYNONYMOUS TO LEGACY OR 1394-A. NOT ASSERTING THIS MEANS THAT THE PORT WILL OPERATE IN BILINGUALLY, SUPPORTING BETA (1394-B) AND LEGACY MODES. PULLING-UP THE UNUSED PORT SAVES A BIT OF POWER AS BETA TONING USES A CLOCK.

NOSTUFF NOSTUFF
R4260 10K 5% 1/16W MF-LF 402
R4261 10K 5% 1/16W MF-LF 402
R4262 10K 5% 1/16W MF-LF 402

FW643 DECOUPLING

NOTE: PLACE 1 CAP CLOSE TO EACH POWER PIN ON U4000

=PP3V3_S5_FW
7MA I/O

C4250 1UF 10% 6.3V CERM 402
C4251 1UF 10% 6.3V CERM 402
C4252 1UF 10% 6.3V CERM 402
C4253 1UF 10% 6.3V CERM 402
C4254 1UF 10% 6.3V CERM 402

=PP3V3_S5_FW
0MA VREG PWR

C4290 0.1UF 10% 16V X7R-CERM 402
C4291 1UF 10% 6.3V CERM 402

NOTE: PLACE THESE NEAR U4000 PIN K12

PP1V0_S5_FW_DVDD

C4260 1UF 10% 6.3V CERM 402
C4261 1UF 10% 6.3V CERM 402
C4262 1UF 10% 6.3V CERM 402
C4263 1UF 10% 6.3V CERM 402
C4264 1UF 10% 6.3V CERM 402
C4265 1UF 10% 6.3V CERM 402
C4266 1UF 10% 6.3V CERM 402

PP3V3_S5_FW_AVDD1

C4240 1UF 10% 6.3V CERM 402
C4241 1UF 10% 6.3V CERM 402
C4242 1UF 10% 6.3V CERM 402

PP3V3_S5_FW_AVDD2

C4280 1UF 10% 6.3V CERM 402

PP1V0_S5_FW_AVDD

C4281 1UF 10% 6.3V CERM 402
C4230 1UF 10% 6.3V CERM 402
C4231 1UF 10% 6.3V CERM 402

FW 3.3V FILTERING

=PP3V3_S5_FW

L4210
120-OHM-0.3A-EMI
0402-LF

PP3V3_S5_FW_AVDD1
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
114MA FIREWIRE PHY

L4211
120-OHM-0.3A-EMI
0402-LF

PP3V3_S5_FW_AVDD2
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
17MA PCIE SERDES

FW PCIE ALIASES

TP_PCIE_FW_R2D_C_N = PCIE_FW_R2D_C_N
TP_PCIE_FW_R2D_C_P = PCIE_FW_R2D_C_P
MAKE_BASE=TRUE

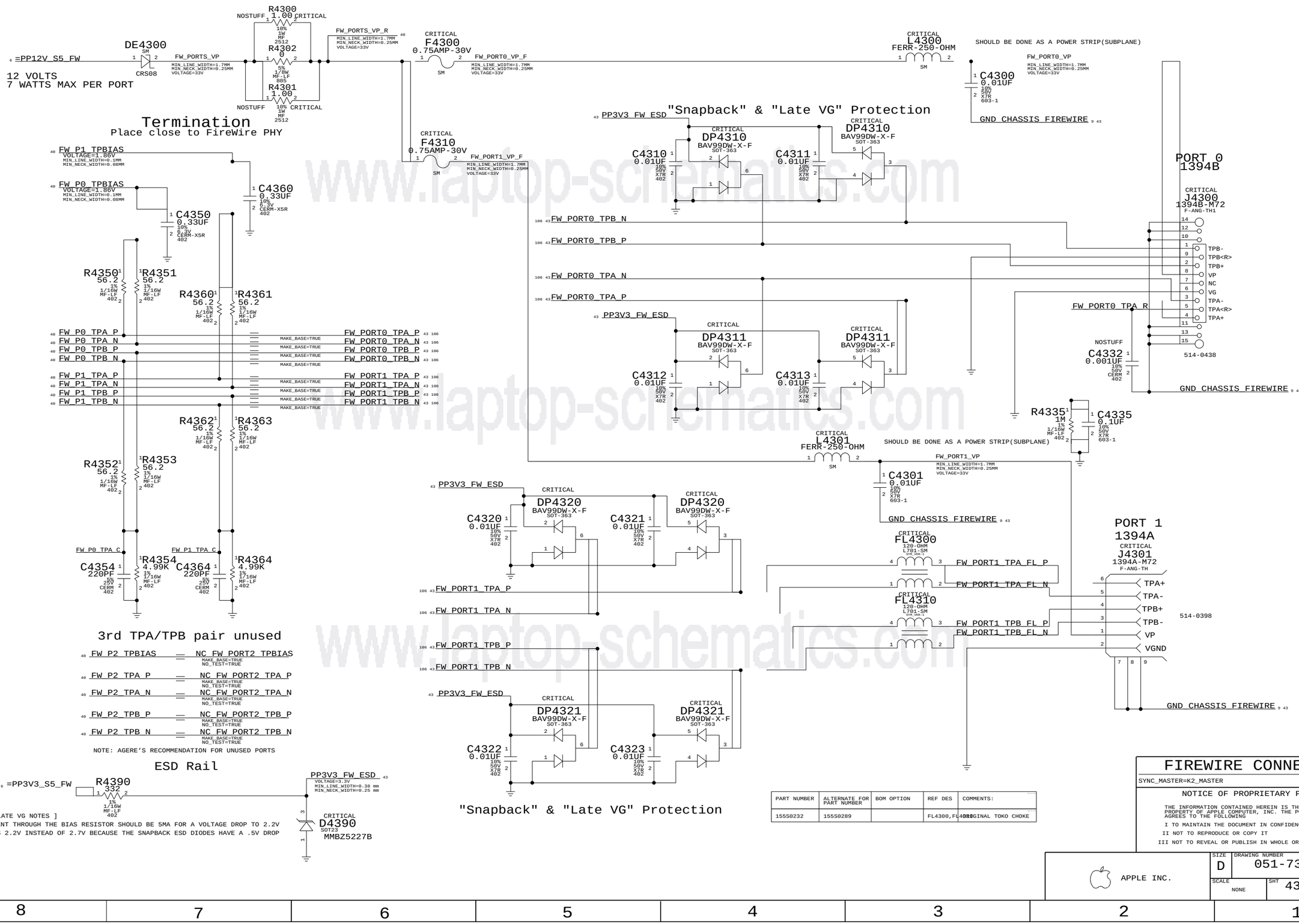
PCIE_FW_D2R_N = TP_PCIE_FW_D2R_N
PCIE_FW_D2R_P = TP_PCIE_FW_D2R_P
MAKE_BASE=TRUE

FW: 1394B MISC

SYNC_MASTER=K2_MASTER
SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 42 OF 118	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		FL4300,FL4310	ORIGINAL TOKO CHOKE

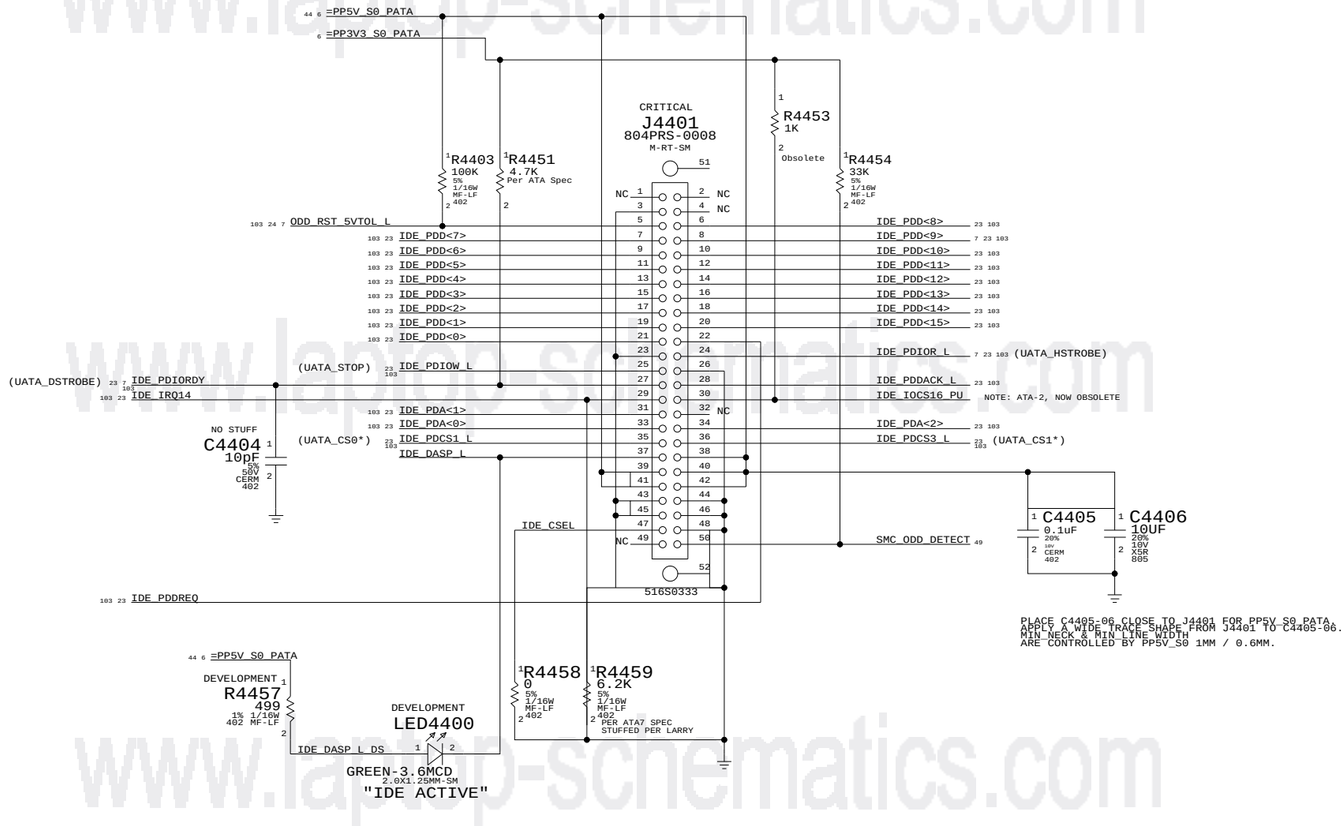
FIREWIRE CONNECTORS

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 43 OF 118	

IDE (ODD) Connector



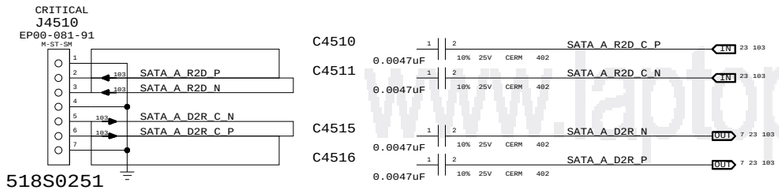
PATA Connector

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

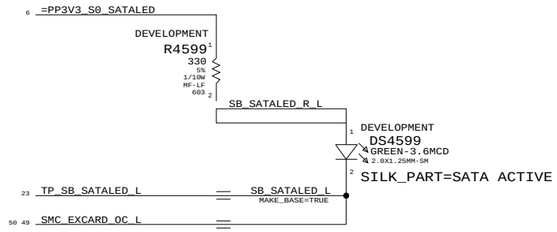
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 44 OF 118	

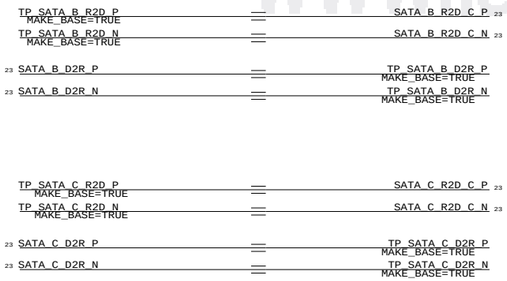
SATA Port A



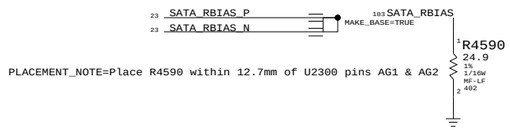
SATA Activity LED



UNUSED SATA PORTS



ICH SATA Support



SATA Connectors

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

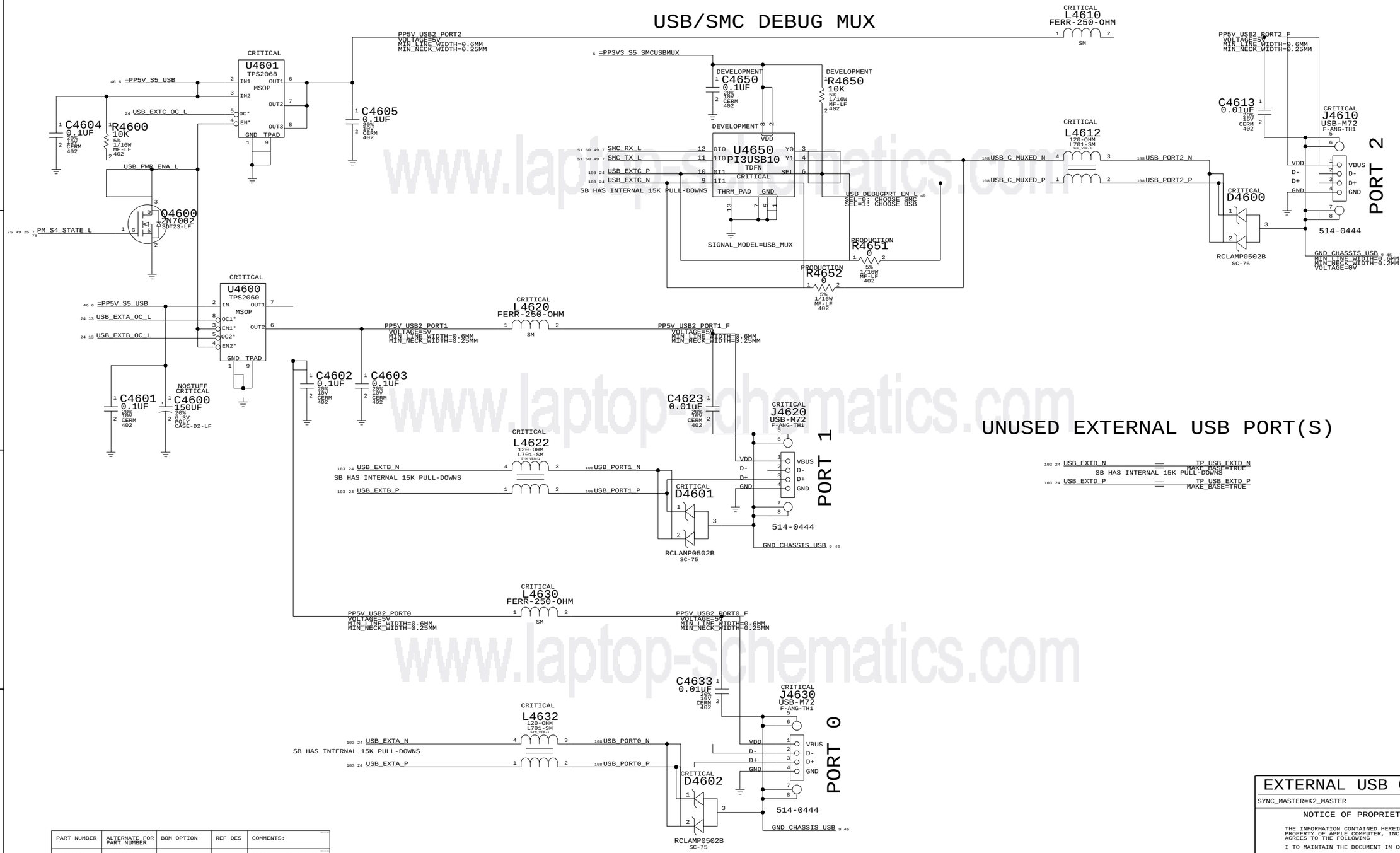
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE

SHT 45 OF 118

USB/SMC DEBUG MUX



UNUSED EXTERNAL USB PORT(S)

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
155S0232	155S0289		ALL	ORIGINAL TOKO CHOKE

EXTERNAL USB CONNECTORS

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 46 OF 118	

CAMERA POWER FILTERING

47 6 =PP5V_S3_BNDI

C4700 10UF 20% 6.3V CERM 805-1

CRITICAL
L4700 FERR-250-OHM SM

PP5V_S3_BNDI
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.2MM
47

C4701 0.1UF 20% 10V CERM 402

LAYOUT NOTE:
PLACE C4700, C4701 & L4700
NEAR J4700 PINS 4 AND 5 IN THE
ORDER LISTED, AND NOT ON
BOTH SIDES OF THE PIN.

K37L (BLUETOOTH) CONNECTOR

CRITICAL
J4720 88262-0401 M-ST-SM

SB HAS INTERNAL 15K PULL-DOWNS

103 24 7 USB_BT_N
103 24 7 USB_BT_P
6 =PP3V3_S3_BT

C4720 10UF 20% 6.3V CERM 805-1

C4721 0.1UF 20% 10V CERM 402

CRITICAL
SDF4721 STDOFF-4.00D6.5H-1.35-2.4-TH

SDF4721_1

R4721 0 5% 1/16W MF-LF 402

CAMERA CONNECTOR

R4701 0 402

L4701 CRITICAL 120-OHM L701-SM

103 24 7 USB_CAMERA_P

SB HAS INTERNAL 15K PULL-DOWNS

NOSTUFF

103 24 7 USB_CAMERA_N

R4702 0 402

108 USB_CAMERA_L_P
108 USB_CAMERA_L_N
47 PP5V_S3_BNDI

FIXME!!! - THIS IS REISTECH CHOKE, T9 USES TOKO(155S0232)

R4710 0 402

L4710 CRITICAL 120-OHM L701-SM

103 24 7 USB_IR_N

SB HAS INTERNAL 15K PULL-DOWNS

NOSTUFF

103 24 7 USB_IR_P

R4711 0 402

USB_IR_L_N 47 108
USB_IR_L_P 47 108

CRITICAL
J4700 88262-0501 M-ST-SM

518S0553

47 CHASSIS_GND_BNDI

47 CHASSIS_GND_BNDI — MAKE_BASE=TRUE

UNUSED INTERNAL USB PORTS

103 24 USB_TPAD_N — TP_USB_TPAD_N MAKE_BASE=TRUE
103 24 USB_TPAD_P — TP_USB_TPAD_P MAKE_BASE=TRUE

SB HAS INTERNAL 15K PULL-DOWNS

103 24 USB_EXCARD_N — TP_USB_EXCARD_N MAKE_BASE=TRUE
103 24 USB_EXCARD_P — TP_USB_EXCARD_P MAKE_BASE=TRUE

SB HAS INTERNAL 15K PULL-DOWNS

IR RECEIVER

CRITICAL
J4780 88262-0401 M-ST-SM

108 47 USB_IR_L_N
108 47 USB_IR_L_P
47 6 =PP5V_S3_BNDI

C4781 1UF 10% 6.3V CERM 402

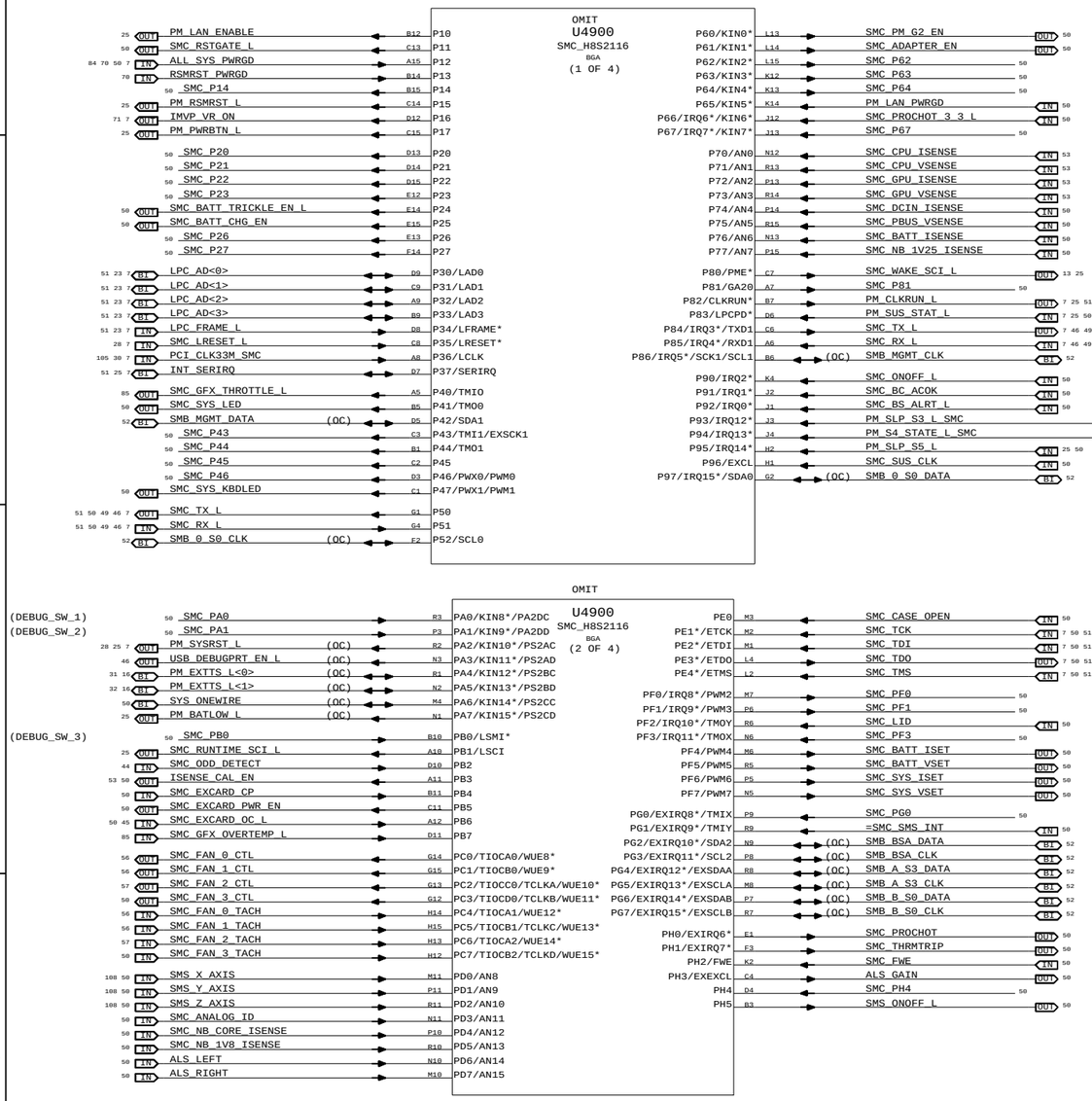
Internal USB Connections

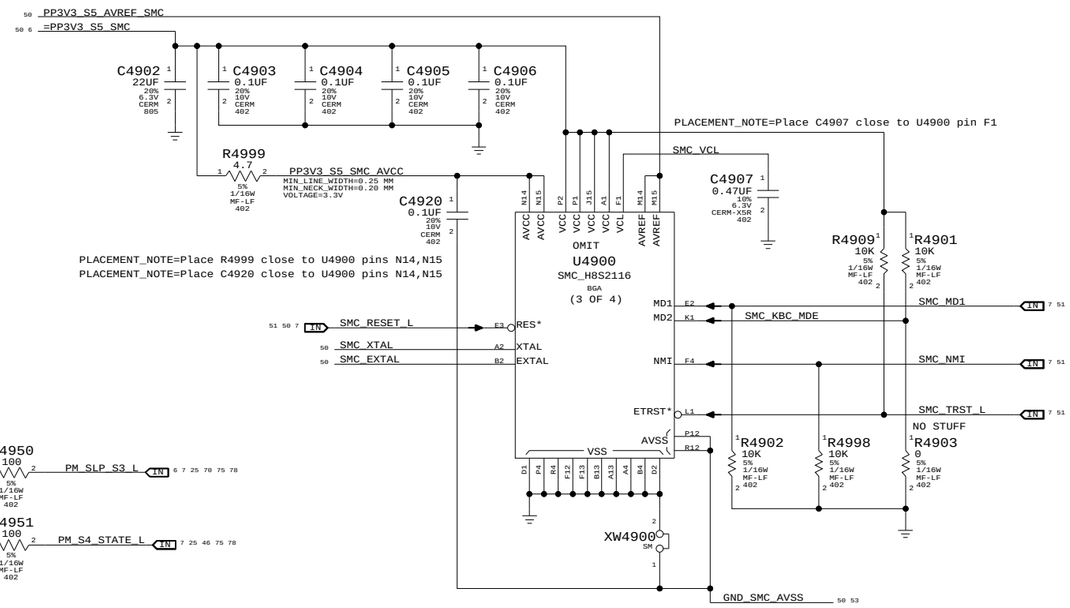
SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

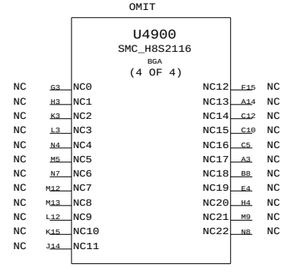
SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 47 OF 118	

NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.



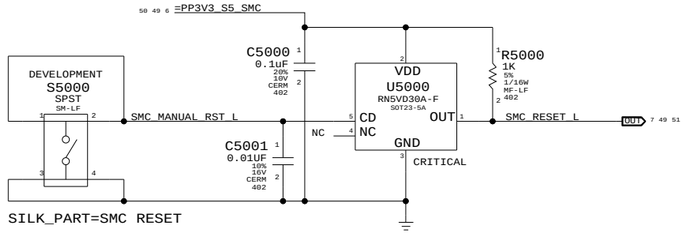
SMC

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=12/15/2006

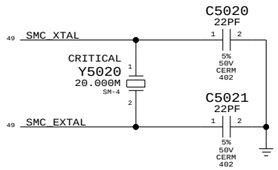
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 49 OF 118	

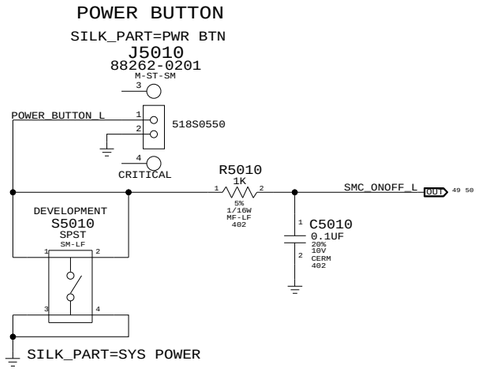
SMC Reset Button / Brownout Detect



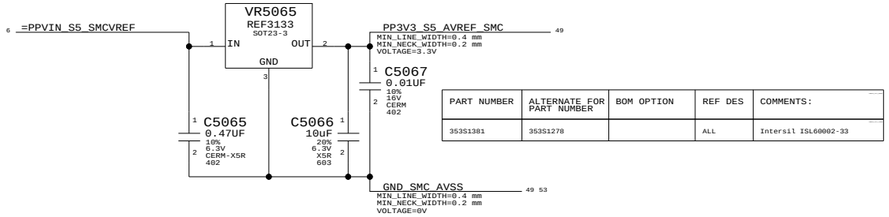
SMC Crystal Circuit



POWER BUTTON



SMC AVREF Supply



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S1381	353S1278		ALL	Intersil ISL60002-33

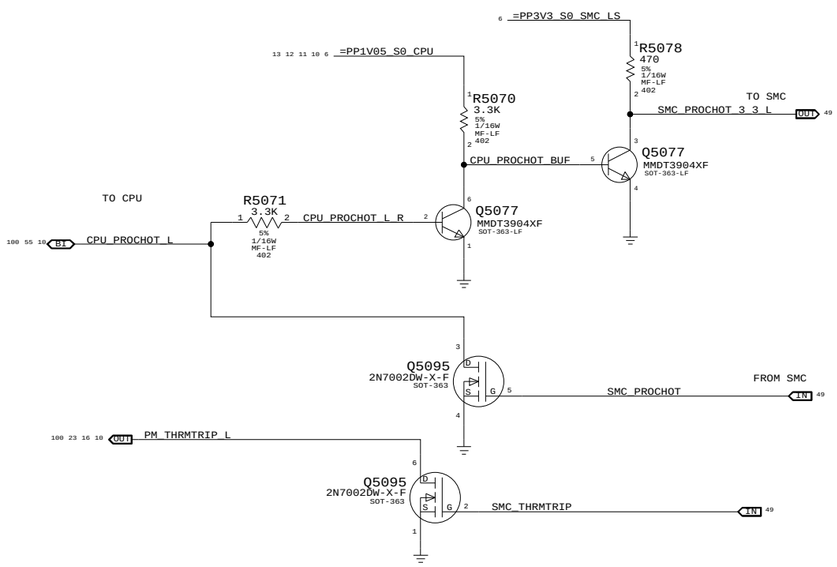
UNUSED TP/NC ALIASES

49 SMC_BATT_ISET	NC_SMC_BATT_ISET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_SYS_ISET	NC_SMC_SYS_ISET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_BATT_VSET	NC_SMC_BATT_VSET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_SYS_VSET	NC_SMC_SYS_VSET	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN	MAKE_BASE=TRUE	NO_TEST=TRUE
108 49 SMS_X_AXIS	NC_SMS_X_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
108 49 SMS_Y_AXIS	NC_SMS_Y_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
108 49 SMS_Z_AXIS	NC_SMS_Z_AXIS	MAKE_BASE=TRUE	NO_TEST=TRUE
49 ALS_GAIN	NC_ALS_GAIN	MAKE_BASE=TRUE	
49 ALS_LEFT	TP_ALS_LEFT	MAKE_BASE=TRUE	
49 ALS_RIGHT	TP_ALS_RIGHT	MAKE_BASE=TRUE	
49 SMC_P14	TP_SMC_P14	MAKE_BASE=TRUE	
49 SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	
49 SMC_P21	TP_SMC_P21	MAKE_BASE=TRUE	
49 SMC_P22	TP_SMC_P22	MAKE_BASE=TRUE	
49 SMC_P23	TP_SMC_P23	MAKE_BASE=TRUE	
49 SMC_P26	TP_SMC_P26	MAKE_BASE=TRUE	
49 SMC_P27	TP_SMC_P27	MAKE_BASE=TRUE	
49 SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE	
49 SMC_P44	TP_SMC_P44	MAKE_BASE=TRUE	
49 SMC_P45	TP_SMC_P45	MAKE_BASE=TRUE	
49 SMC_P62	TP_SMC_P62	MAKE_BASE=TRUE	
49 SMC_P63	TP_SMC_P63	MAKE_BASE=TRUE	
49 SMC_P64	TP_SMC_P64	MAKE_BASE=TRUE	
49 SMC_P81	TP_SMC_P81	MAKE_BASE=TRUE	
49 SMC_PF0	TP_SMC_PF0	MAKE_BASE=TRUE	
49 SMC_PF1	TP_SMC_PF1	MAKE_BASE=TRUE	
49 SMC_FAN_3_CTL	TP_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
49 SMC_FAN_3_TACH	TP_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
49 SMC_PM_G2_EN	TP_SMC_PM_G2_EN	MAKE_BASE=TRUE	
49 SMC_ADAPTER_EN	TP_SMC_ADAPTER_EN	MAKE_BASE=TRUE	
49 SMC_SYS_KBDLED	TP_SMC_SYS_KBDLED	MAKE_BASE=TRUE	
49 SMC_SYS_LED	TP_SMC_SYS_LED	MAKE_BASE=TRUE	
49 SMC_EXCARD_PWR_EN	TP_SMC_EXCARD_PWR_EN	MAKE_BASE=TRUE	
49 SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	
49 SMS_ONOFF_L	TP_SMS_ONOFF_L	MAKE_BASE=TRUE	
49 SMC_P46	TP_SMC_P46	MAKE_BASE=TRUE	

ANALOG SENSORS

49 SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_NB_CORE_ISENSE	NC_SMC_NB_CORE_ISENSE	MAKE_BASE=TRUE	NO_TEST=TRUE
49 SMC_DCIN_ISENSE	SMC_12V_S0_ISENSE	MAKE_BASE=TRUE	53
49 SMC_PBUS_VSENSE	SMC_12V_S0_VSENSE	MAKE_BASE=TRUE	53
49 SMC_BATT_ISENSE	SMC_12V_S5_ISENSE	MAKE_BASE=TRUE	53
49 SMC_NB_1V25_ISENSE	SMC_12V_S5_VSENSE	MAKE_BASE=TRUE	53

SMC FSB to 3.3V Level Shifting



MISC. SIGNAL ALIASES

49 SMC_ANALOG_ID	ACDC_TEMP	MAKE_BASE=TRUE	6
49 SMC_SUS_CLK	SUS_CLK_SB	MAKE_BASE=TRUE	25
49 PM_LAN_PWRGD	ALL_SYS_PWRGD	MAKE_BASE=TRUE	7 49 70 84

50 49 6 =PP3V3_S5_SMC

50 49 SMC_ONOFF_L	R5032	10K	5%	1/16W	MF-LF	402	
49 SMC_LID	R5033	100K	5%	1/16W	MF-LF	402	
49 SMC_FWE	R5034	10K	5%	1/16W	MF-LF	402	
51 49 46 7 SMC_TX_L	R5035	10K	5%	1/16W	MF-LF	402	
51 49 46 7 SMC_RX_L	R5036	100K	5%	1/16W	MF-LF	402	
49 SYS_ONEWIRE	R5037	2.0K	5%	1/16W	MF-LF	402	
49 SMC_BS_ALRT_L	R5038	100K	5%	1/16W	MF-LF	402	
51 49 7 SMC_TMS	R5039	10K	5%	1/16W	MF-LF	402	
51 49 7 SMC_TDO	R5040	10K	5%	1/16W	MF-LF	402	
51 49 7 SMC_TDI	R5041	10K	5%	1/16W	MF-LF	402	
51 49 7 SMC_TCK	R5042	10K	5%	1/16W	MF-LF	402	
49 45 SMC_EXCARD_OC_L NO STUFF	R5043	10K	5%	1/16W	MF-LF	402	
49 SMC_PF3	R5080	10K	5%	1/16W	MF-LF	402	
49 SMC_PH4	R5082	10K	5%	1/16W	MF-LF	402	
49 SMC_BC_ACOK	R5047	10K	5%	1/16W	MF-LF	402	
49 SMC_PA0	R5096	10K	5%	1/16W	MF-LF	402	
49 SMC_PA1	R5090	10K	5%	1/16W	MF-LF	402	
49 SMC_PB0	R5091	10K	5%	1/16W	MF-LF	402	
49 =SMC_SMS_INT SMC_SMS_INT MAKE_BASE=TRUE	R5092	10K	5%	1/16W	MF-LF	402	
49 SMC_P67	R5093	10K	5%	1/16W	MF-LF	402	
49 SMC_PG0	R5094	10K	5%	1/16W	MF-LF	402	
			5%	1/16W	MF-LF	402	
49 SMC_CASE_OPEN	R5046	10K	5%	1/16W	MF-LF	402	
49 SMC_EXCARD_CP	R5048	10K	5%	1/16W	MF-LF	402	
51 49 25 7 PM_SUS_STAT_L	R5083	100K	5%	1/16W	MF-LF	402	
49 25 PM_SLP_S5_L	R5084	100K	5%	1/16W	MF-LF	402	
53 49 ISENSE_CAL_EN NO STUFF	R5088	100K	5%	1/16W	MF-LF	402	

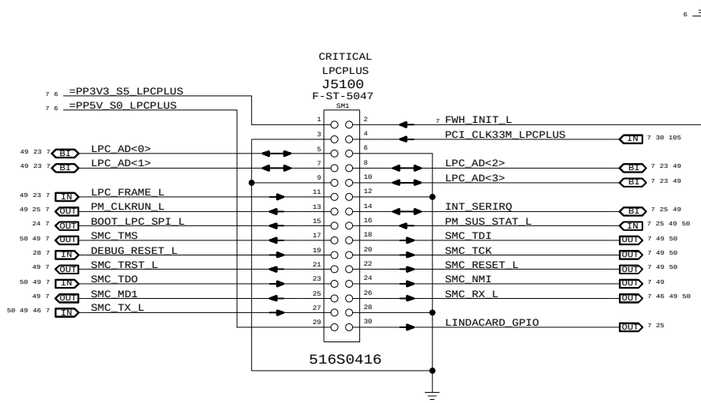
SMC Support

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

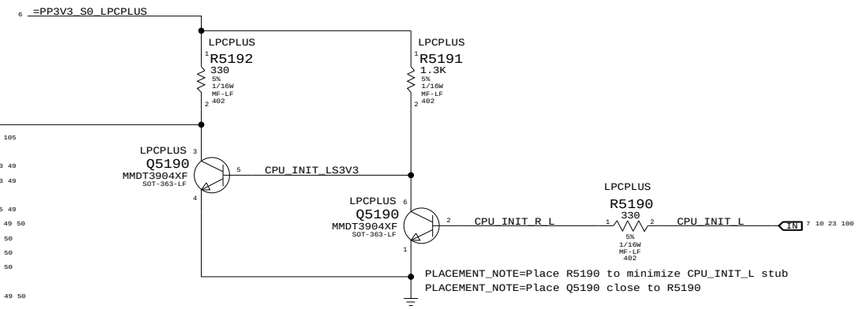
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 50 OF 118	

LPC+ Connector



FWH_INIT_L Generation



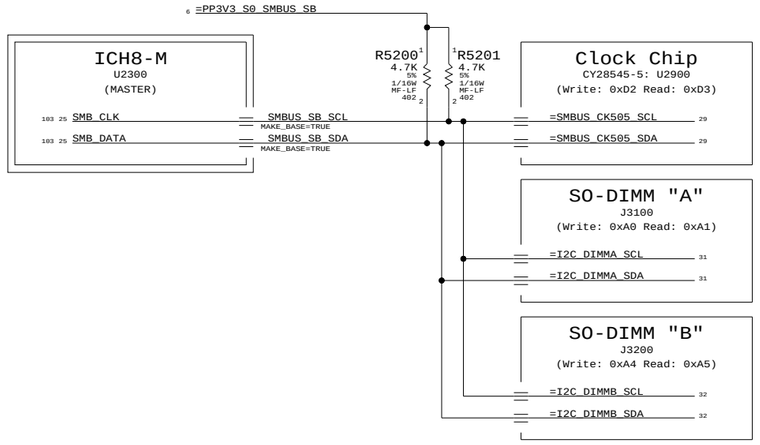
LPC+ Debug Connector

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=06/08/2007

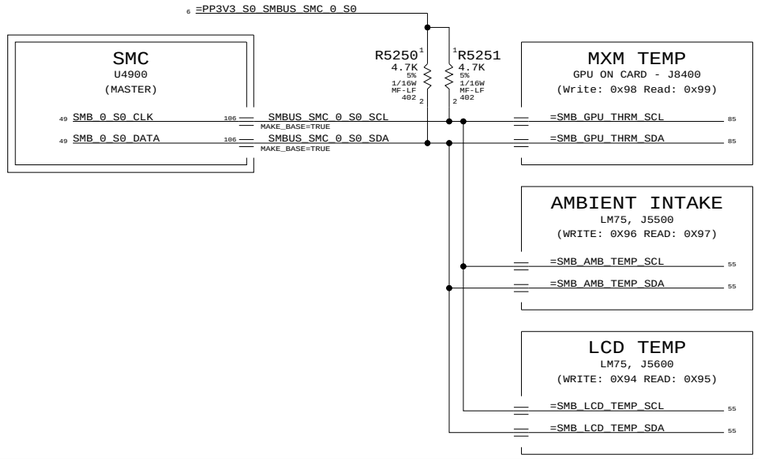
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 51 OF 118	

ICH8-M SMBus Connections

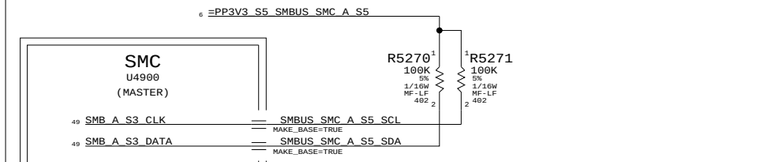


SMC "0" SMBus Connections

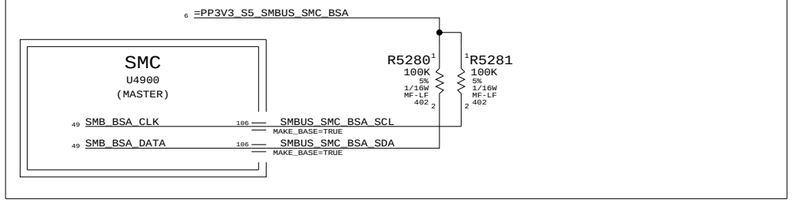


SMC "A" SMBus Connections

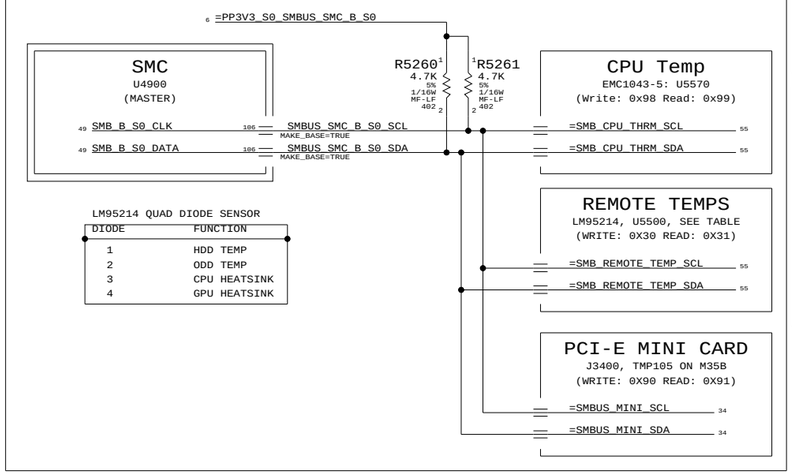
NOTE: SMC RMT BUS REMAINS POWERED AND MAY BE ACTIVE IN S5 STATE



UNUSED SMC "BATTERY A" SMBUS CONNECTIONS



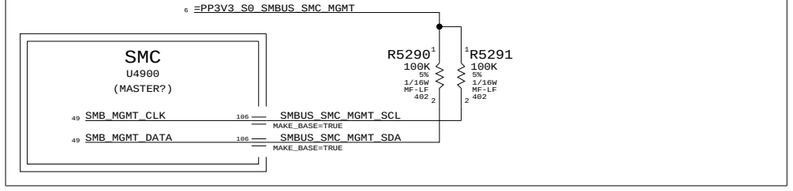
SMC "B" SMBus Connections



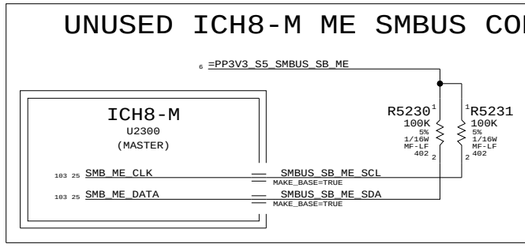
LM95214 QUAD DIODE SENSOR

DIODE	FUNCTION
1	HDD TEMP
2	ODD TEMP
3	CPU HEATSINK
4	GPU HEATSINK

UNUSED SMC "MANAGEMENT" SMBUS CONNECTIONS



UNUSED ICH8-M ME SMBUS CONNECTIONS



SMBUS CONNECTIONS

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

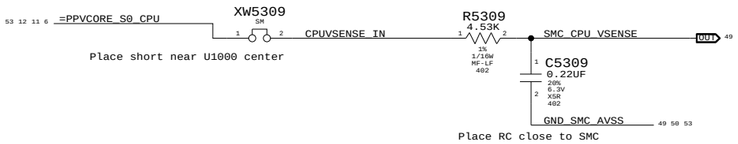
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 52 OF 118	

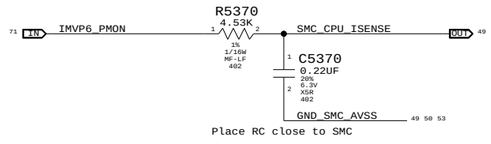
CPU POWER SENSE CALIBRATION CIRCUIT

Switches in fixed load on power supplies to calibrate current sense circuits

CPU Voltage Sense / Filter



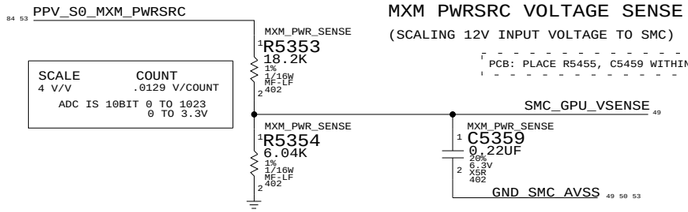
CPU SUPPLY POWER SENSE FILTER



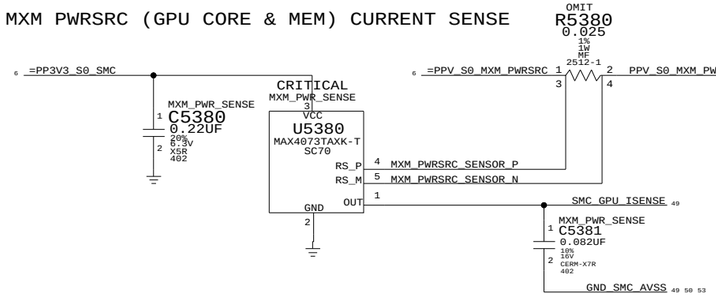
PCPU = VPMON / (17.5 * .0021)

MXM PWRSRC VOLTAGE SENSE

(SCALING 12V INPUT VOLTAGE TO SMC)



MXM PWRSRC (GPU CORE & MEM) CURRENT SENSE



K2 SET FOR APPROX 2V AT 4A ON PWRSRC

SCALE	COUNT
2 A/V	.0064453 A/COUNT

ADC IS 10BIT 0 TO 1023, 0 TO 3.3V

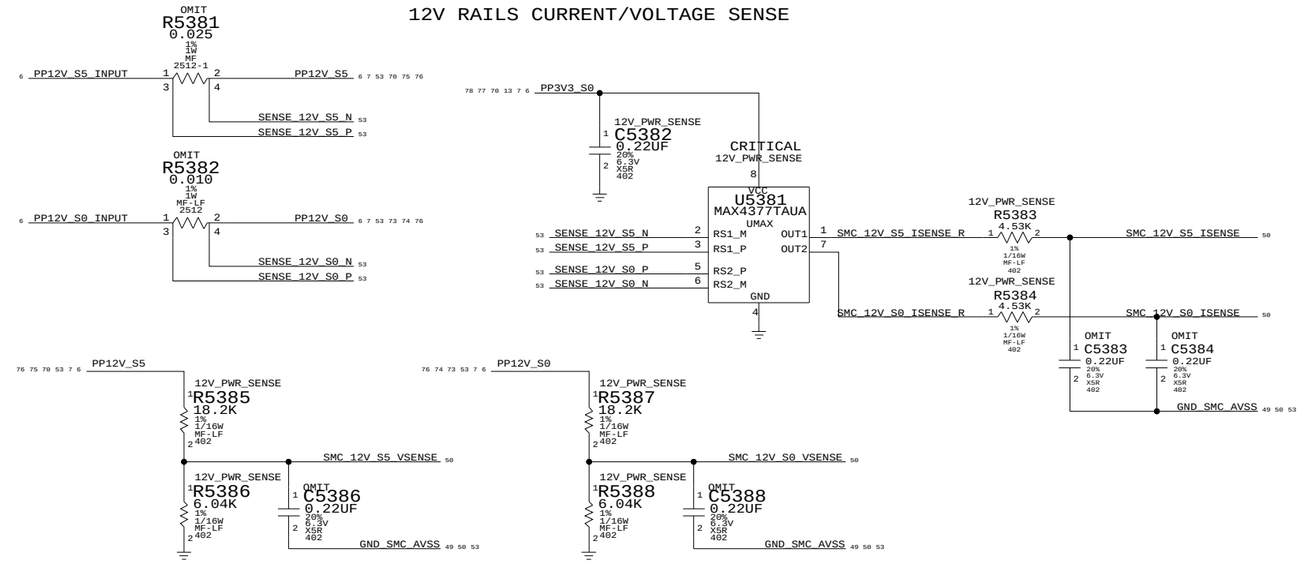
K3 SET FOR APPROX 1.98V AT 5.5A ON PWRSRC

SCALE	COUNT
2.778 A/V	.0087518 A/COUNT

ADC IS 10BIT 0 TO 1023, 0 TO 3.3V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0063	1	25 MILLIOHM	R5380	CRITICAL	20_INCH_LCD
107S0111	1	18 MILLIOHM	R5380	CRITICAL	24_INCH_LCD

12V RAILS CURRENT/VOLTAGE SENSE

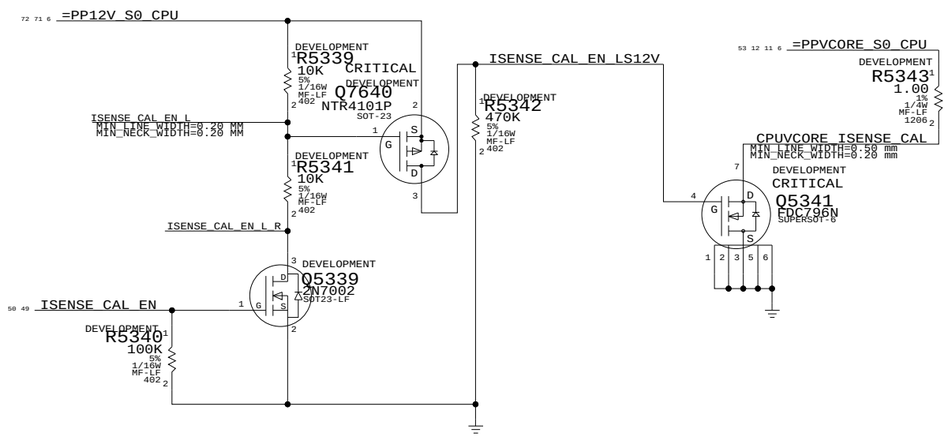


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0069	1	10 MILLIOHM	R5382	CRITICAL	K2_BETTER
107S0112	1	8 MILLIOHM	R5382	CRITICAL	24_INCH_LCD
107S0070	1	RES,0 OHM,2512	R5382	CRITICAL	K2_GOOD
107S0063	1	25 MILLIOHM	R5381	CRITICAL	12V_PWR_SENSE
107S0070	1	RES,0 OHM,2512	R5381	CRITICAL	K2_GOOD
116S0090	4	RES,10K0HM,5%,402	C5383,C5384,C5386,C5388		K2_GOOD
132S0080	4	CAP,22UF,20%,6.3V,X5R,402	C5383,C5384,C5386,C5388		12V_PWR_SENSE

12V_PWR_SENSE SHOULD BE STUFFED FOR K2 BETTER AND K3 (BEST/CTO)
K2 GOOD WILL NOT HAVE THE SENSORS, SO CAPS FROM THE RC FILTER BECOME RESISTORS TO GROUND (SO SMC READS 0)

K2 GOOD DOES NOT NEED 12V POWER SENSE BECAUSE THE CONFIGURATION DOES NOT DRAW CURRENT WHICH APPROACHES THE ACDC SPEC

ISENSE_CAL_EN_LS12V

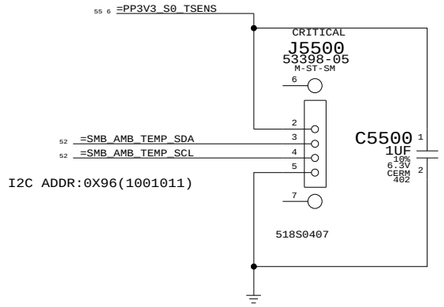


Current & Voltage Sensing	
SYNC_MASTER=K2_MASTER	SYNC_DATE=N/A

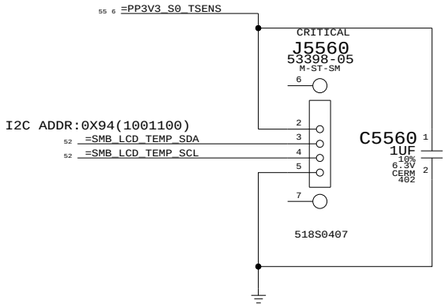
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 53 OF 118	

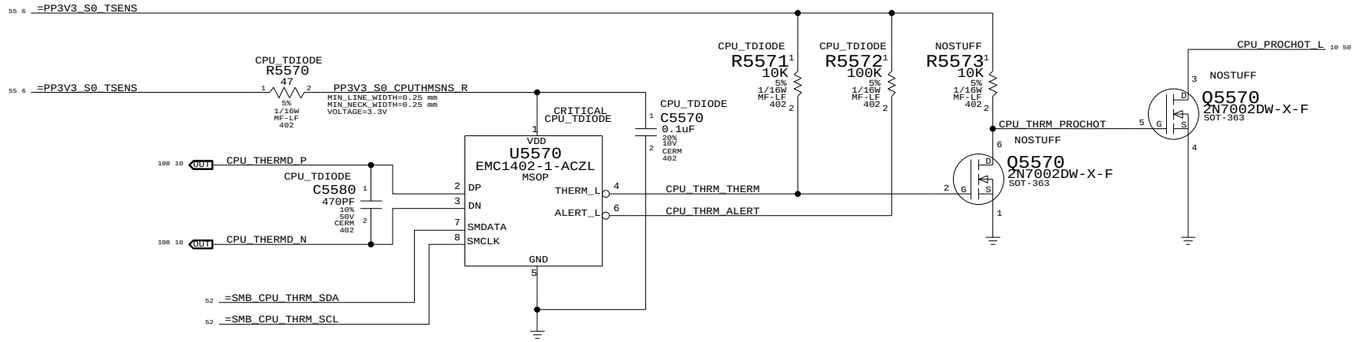
AMBIENT TEMP SENSOR



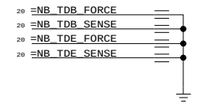
LCD TEMP SENSOR



CPU T-Diode Thermal Sensor



UNUSED NB THERMAL SENSORS

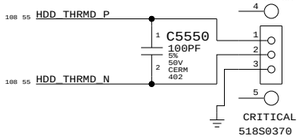


REMOTE THERMAL SENSORS (HEATSINKS AND DISKS)

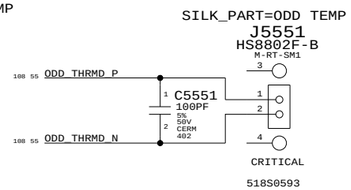
PLACE ALL CAPS NEAR U5500

PLACE DISK SENSOR CONNS BOTTOM SIDE

SILK_PART=HDD TEMP

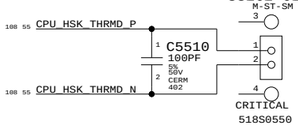


SILK_PART=ODD TEMP

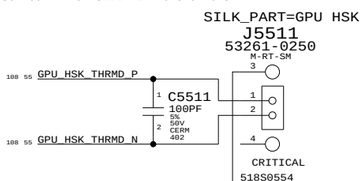


PLACE HSK SENSOR CONN. TOP SIDE NEAR GPU OR CPU

SILK_PART=CPU HSK

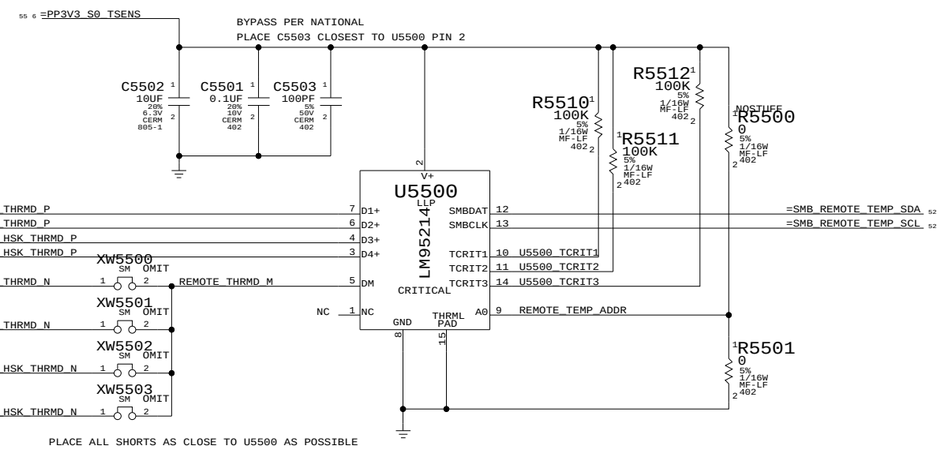


SILK_PART=GPU HSK



TO HELP POWER DELIVERY

74 73 7 6 PPMCH_CORE_S0



PLACE ALL SHORTS AS CLOSE TO U5500 AS POSSIBLE
ROUTE DIODE SIGNALS AS DIFF PAIRS

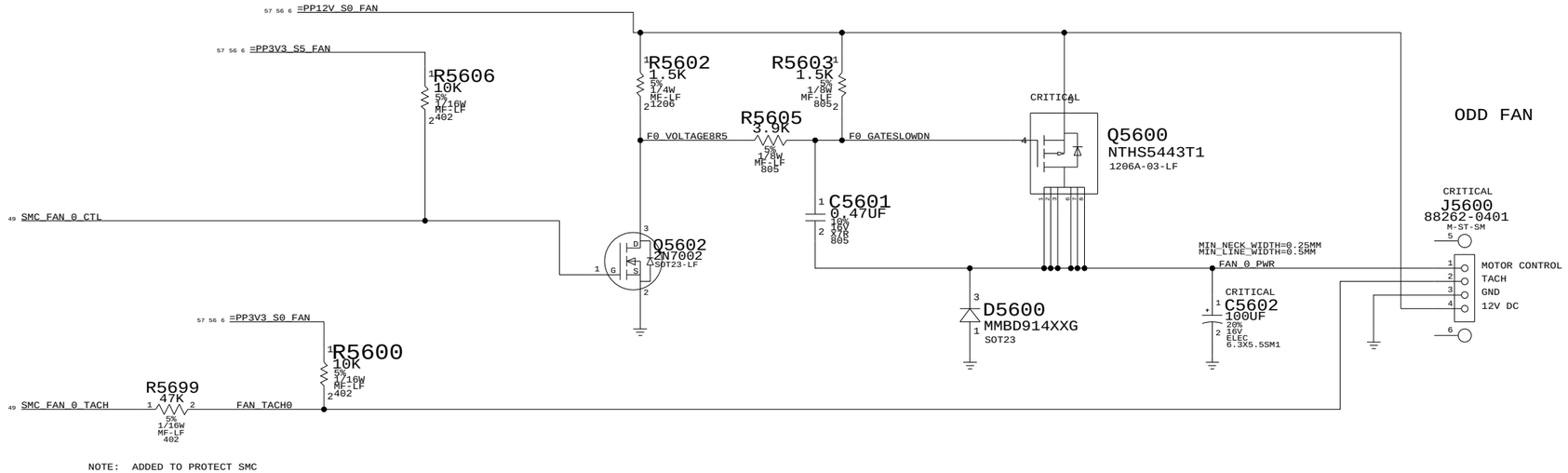
Thermal Sensors

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

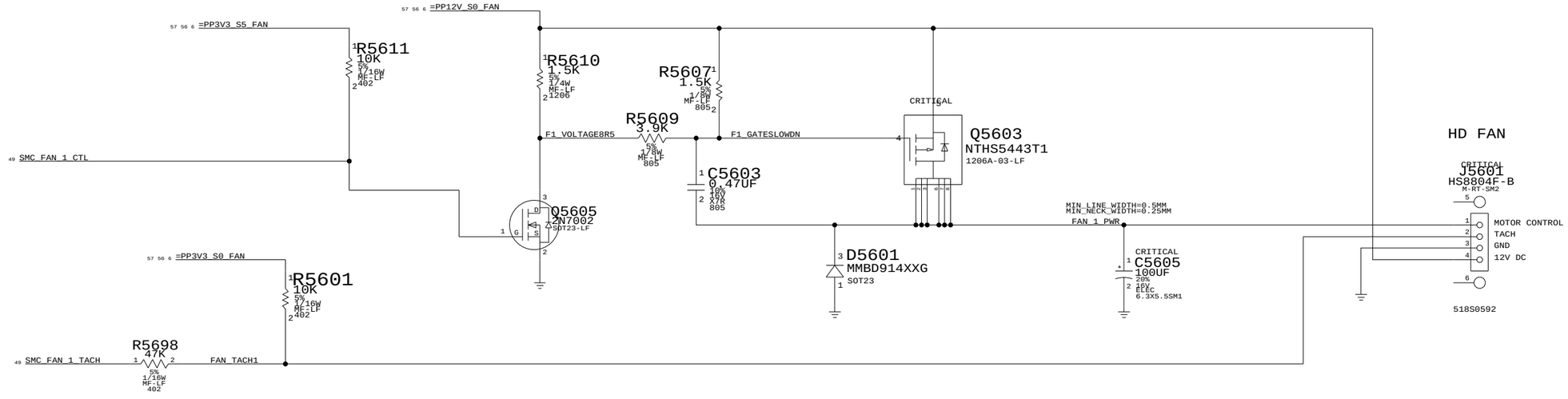
SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 55 OF 118	

FAN 0



NOTE: ADDED TO PROTECT SMC

FAN 1



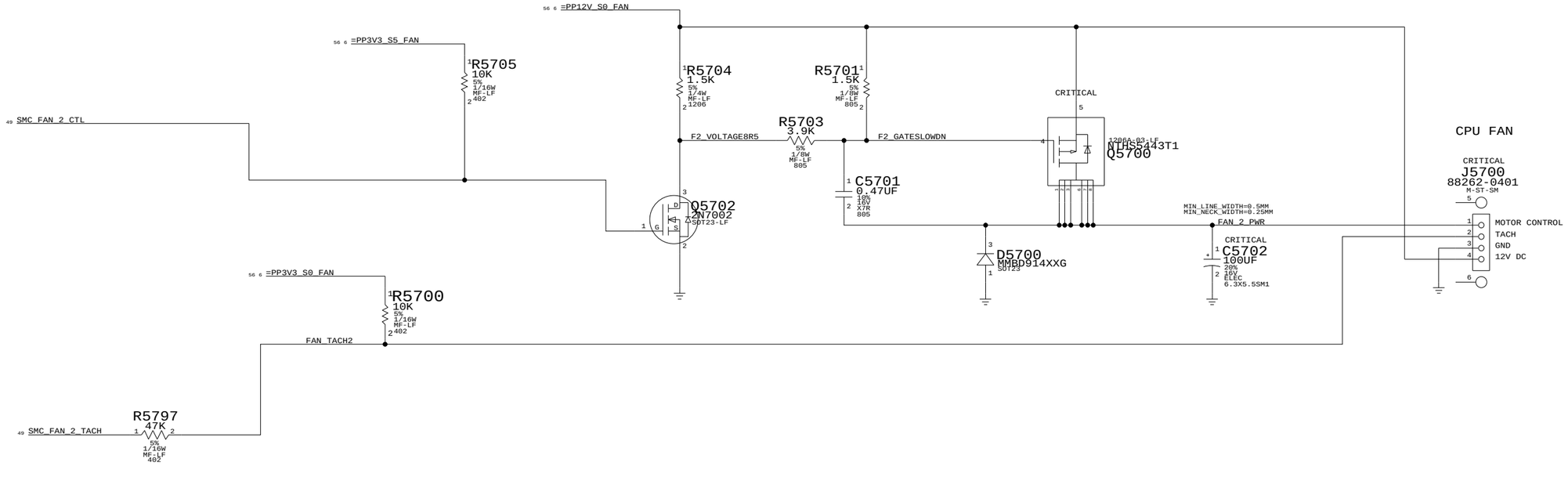
HD AND OD FAN

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

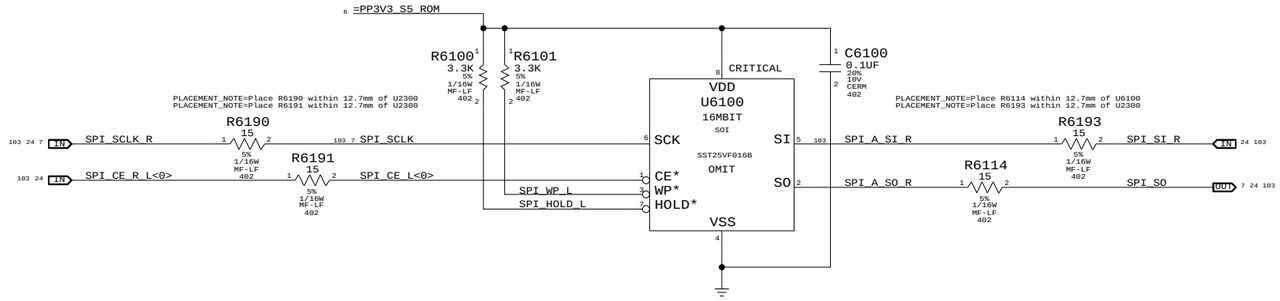
SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 56 OF 118	

FAN 2



CPU FAN		
SYNC_MASTER=K2_MASTER		SYNC_DATE=N/A

APPLE INC.	SIZE D	DRAWING NUMBER 051-7388	REV. A
	SCALE NONE	SHT 57 OF 118	



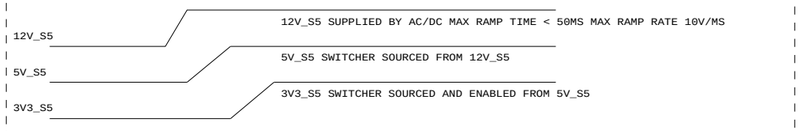
SPI BootROM

SYNC_MASTER=T9_MLB_NOME SYNC_DATE=06/08/2007

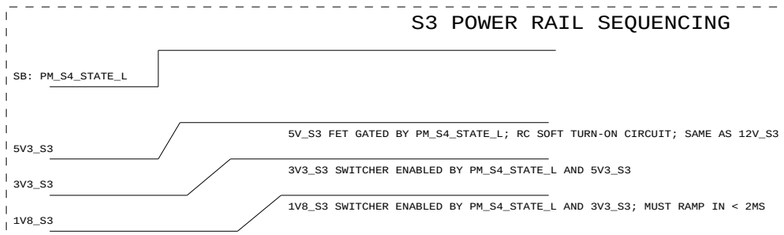
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 61 OF 118	

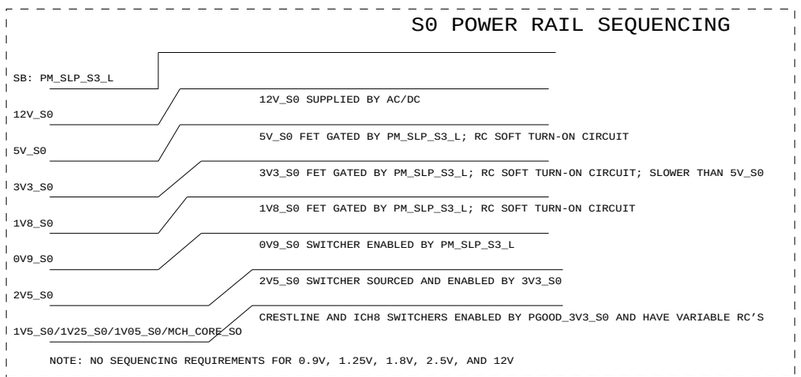
S5 POWER RAIL SEQUENCING



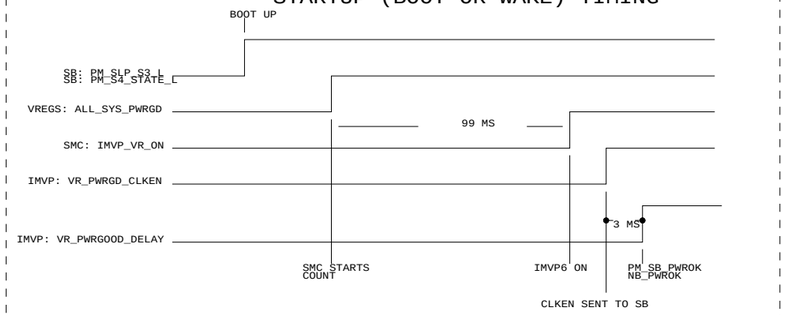
S3 POWER RAIL SEQUENCING



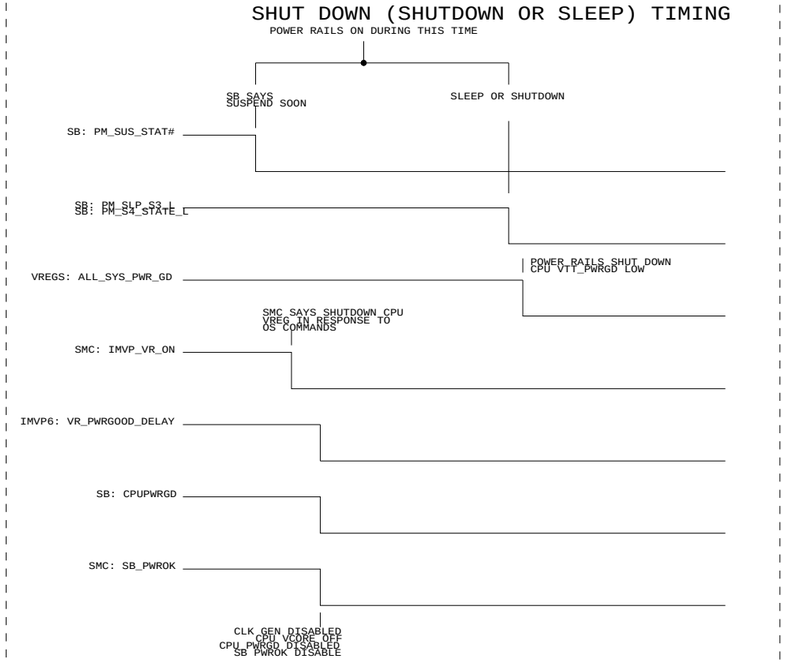
S0 POWER RAIL SEQUENCING



STARTUP (BOOT OR WAKE) TIMING



SHUT DOWN (SHUTDOWN OR SLEEP) TIMING



POWER SEQUENCING BLOCK DIAGRAM

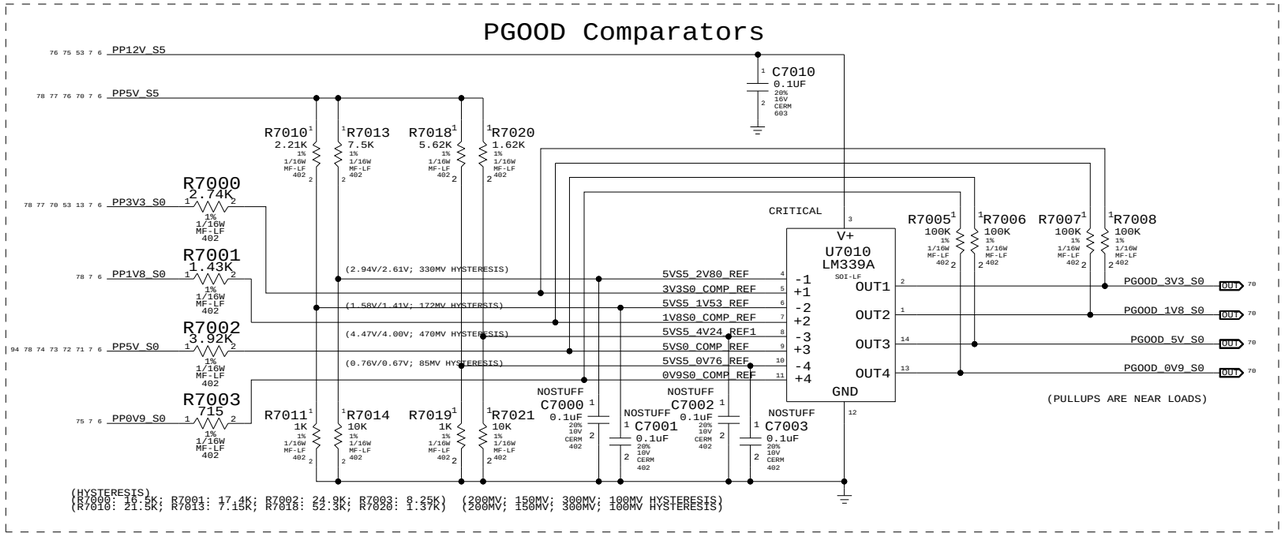
SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

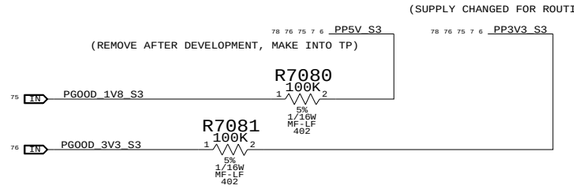
SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE	SHT	OF
NONE	69	118

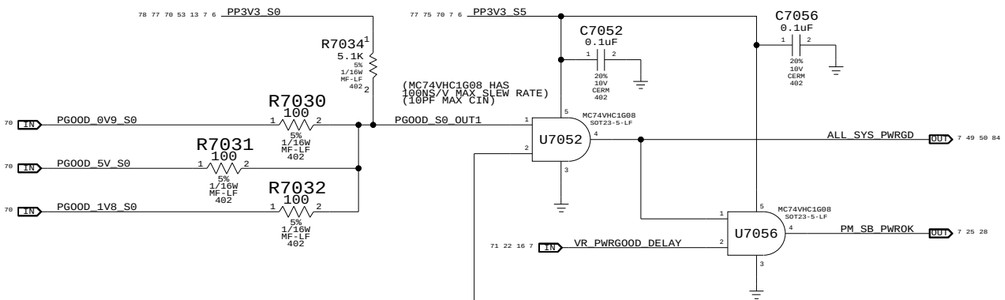
PGOOD Comparators



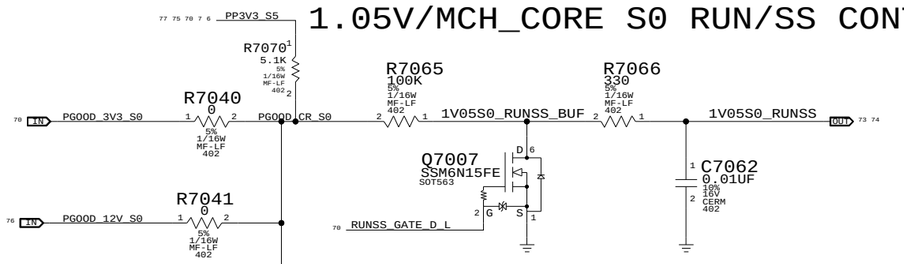
(SUPPLY CHANGED FOR ROUTING)



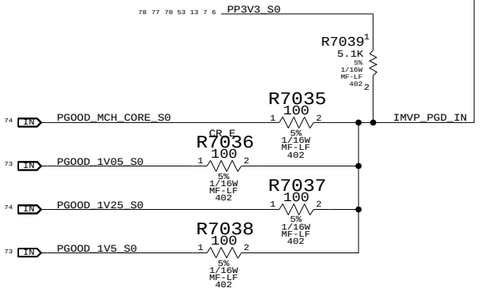
PWROK Sequencing



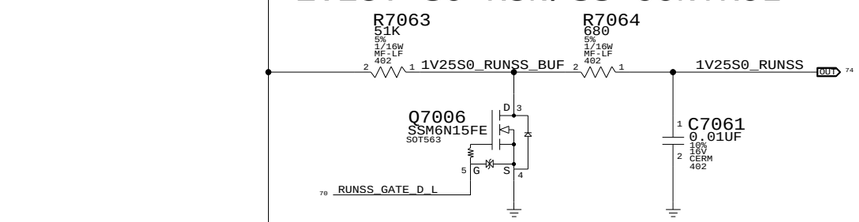
1.05V/MCH_CORE S0 RUN/SS CONTROL

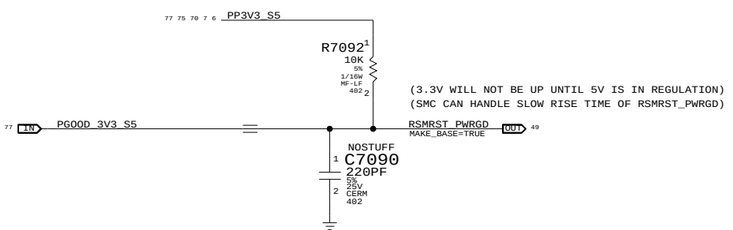


(NOT ALL PGOODS ARE NEEDED HERE SINCE
(SOME REGULATORS ARE DAISY CHAIN ENABLED)

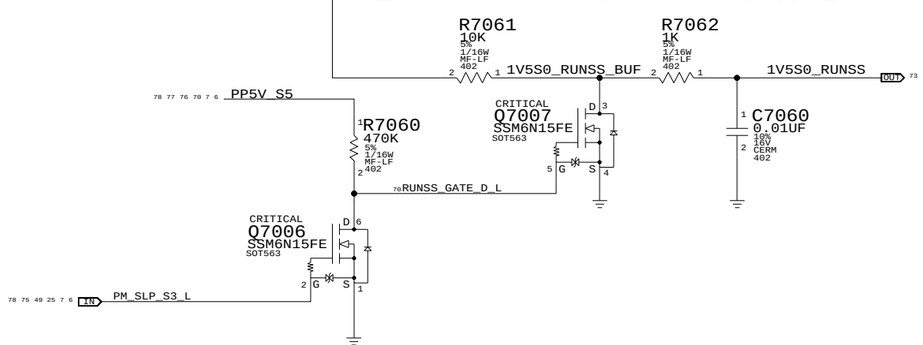


1.25V S0 RUN/SS CONTROL





1.5V S0 RUN/SS CONTROL



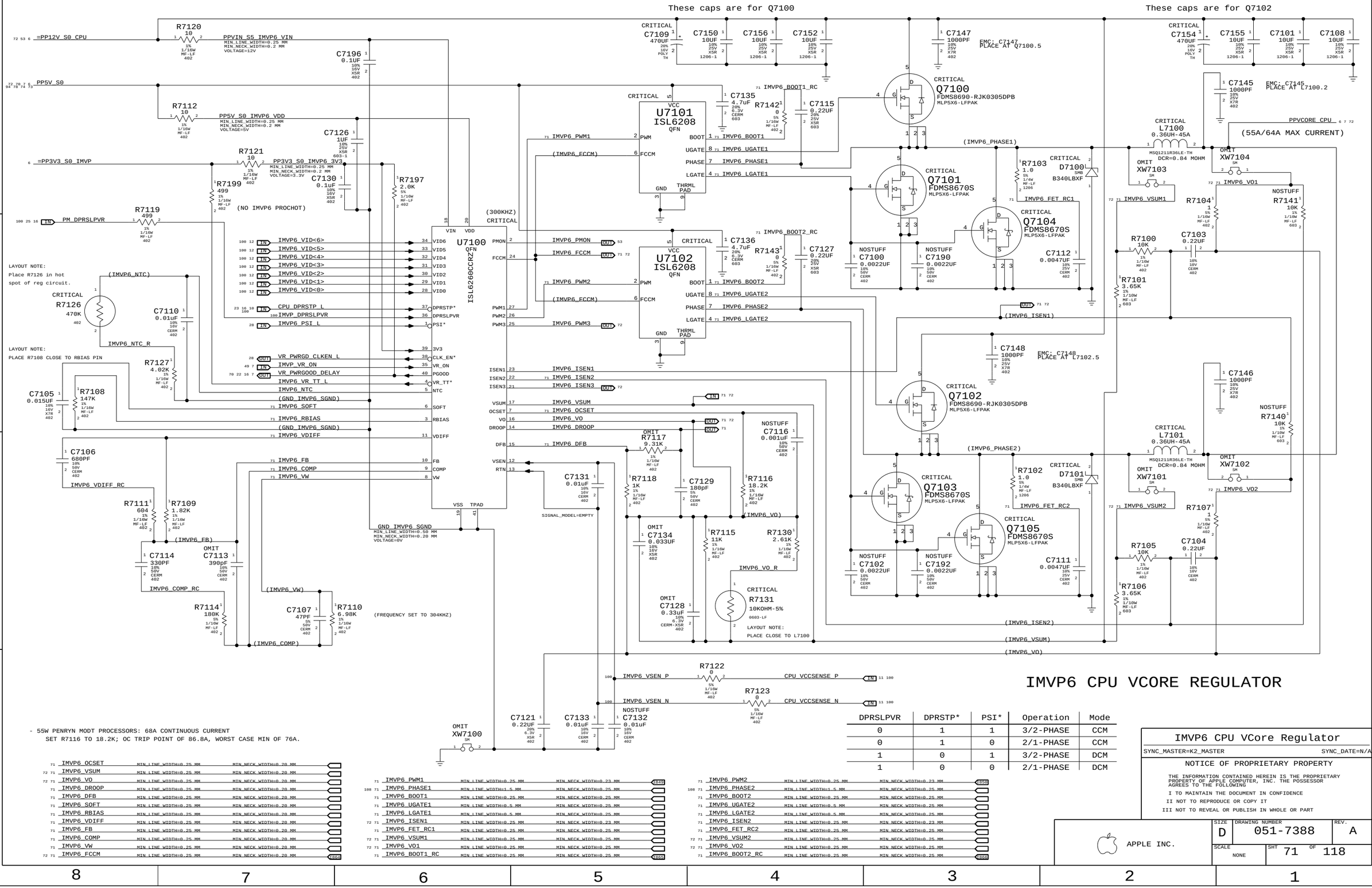
PGOOD and Power Sequencing

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE SHT 70 OF 118



DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	3/2-PHASE	CCM
0	1	0	2/1-PHASE	CCM
1	0	1	3/2-PHASE	DCM
1	0	0	2/1-PHASE	DCM

- 55W PENRYN MODT PROCESSORS: 68A CONTINUOUS CURRENT
  SET R7116 TO 18.2K; OC TRIP POINT OF 86.8A, WORST CASE MIN OF 76A.

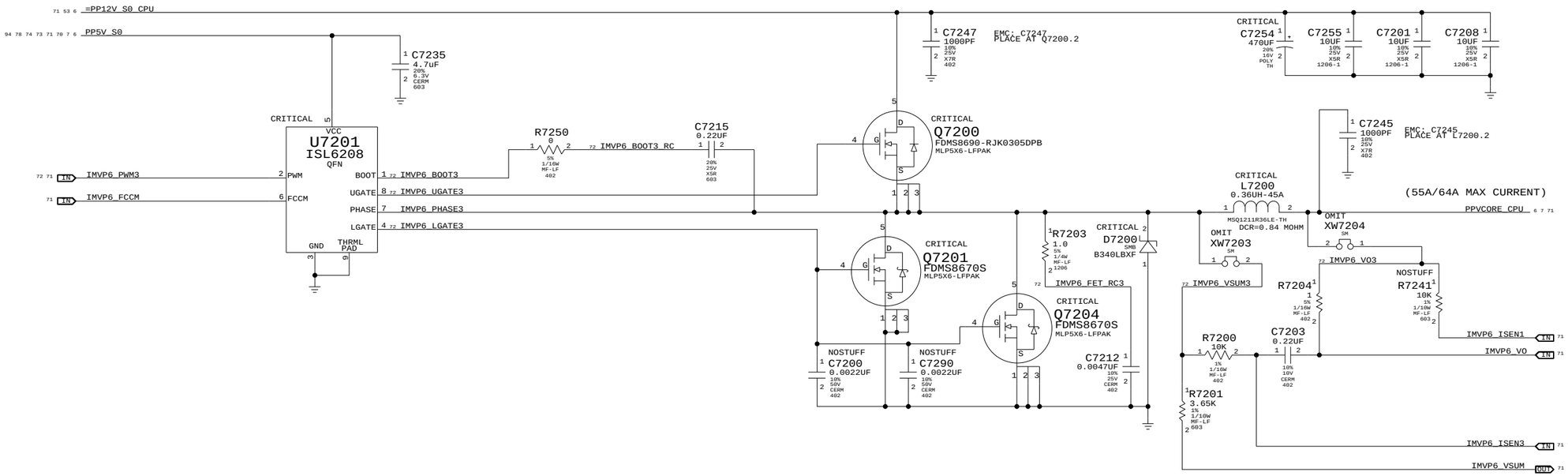
IMVP6_OCSET, IMVP6_VSUM, IMVP6_VO, IMVP6_DROOP, IMVP6_DFB, IMVP6_SOFT, IMVP6_RBIAS, IMVP6_VDIFF, IMVP6_FB, IMVP6_COMP, IMVP6_VW, IMVP6_FCCM — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.20 MM

IMVP6_PWM1, IMVP6_PHASE1, IMVP6_BOOT1, IMVP6_UGATE1, IMVP6_LGATE1, IMVP6_ISEN1, IMVP6_FET_RC1, IMVP6_VSUM1, IMVP6_VO1, IMVP6_BOOT1_RC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.23 MM

IMVP6_PWM2, IMVP6_PHASE2, IMVP6_BOOT2, IMVP6_UGATE2, IMVP6_LGATE2, IMVP6_ISEN2, IMVP6_FET_RC2, IMVP6_VSUM2, IMVP6_VO2, IMVP6_BOOT2_RC — MIN_LINE_WIDTH=0.25 MM, MIN_NECK_WIDTH=0.23 MM

IMVP6 CPU VCore Regulator			
SYNC_MASTER=K2_MASTER	SYNC_DATE=N/A		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE INC.	SIZE D	DRAWING NUMBER 051-7388	REV. A
	SCALE NONE	SHT 71 OF 118	

IMVP6 CPU VCORE REGULATOR



NO TEST FOR CPU VREG, ADDED K2/K3

```
IMVP6_VO1     NO_TEST=TRUE
IMVP6_VO2     NO_TEST=TRUE
IMVP6_VO3     NO_TEST=TRUE
IMVP6_VSUM1   NO_TEST=TRUE
IMVP6_VSUM2   NO_TEST=TRUE
IMVP6_VSUM3   NO_TEST=TRUE
```

```
IMVP6_PWM3       MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.23 MM   T51
IMVP6_PHASE3     MIN_LINE_WIDTH=1.5 MM    MIN_NECK_WIDTH=0.25 MM   T45
IMVP6_BOOT3      MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.25 MM   T44
IMVP6_UGATE3     MIN_LINE_WIDTH=0.5 MM    MIN_NECK_WIDTH=0.25 MM   T46
IMVP6_LGATE3     MIN_LINE_WIDTH=0.5 MM    MIN_NECK_WIDTH=0.25 MM   T48
IMVP6_ISEN3      MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.23 MM   T49
IMVP6_FET_RC3    MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.25 MM   T47
IMVP6_VSUM3      MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.25 MM   T43
IMVP6_VO3        MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.25 MM   T50
IMVP6_BOOT3_RC   MIN_LINE_WIDTH=0.25 MM   MIN_NECK_WIDTH=0.25 MM   T52
```

IMVP6 3RD PHASE

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
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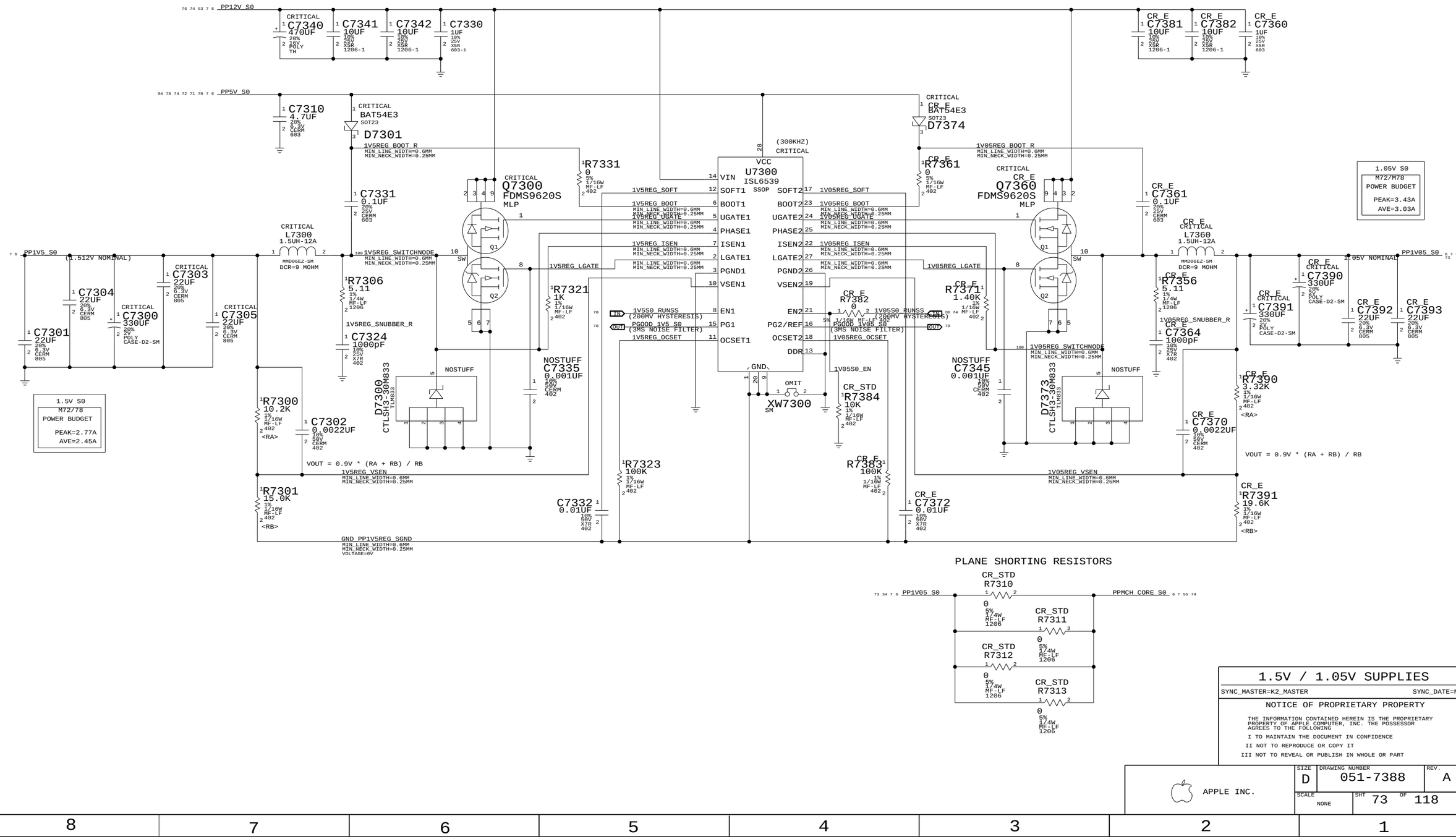
SCALE: NONE	SHT 72 OF 118	

1.5V S0 & 1.05V SO RAILS



PLANE SHORTING RESISTORS

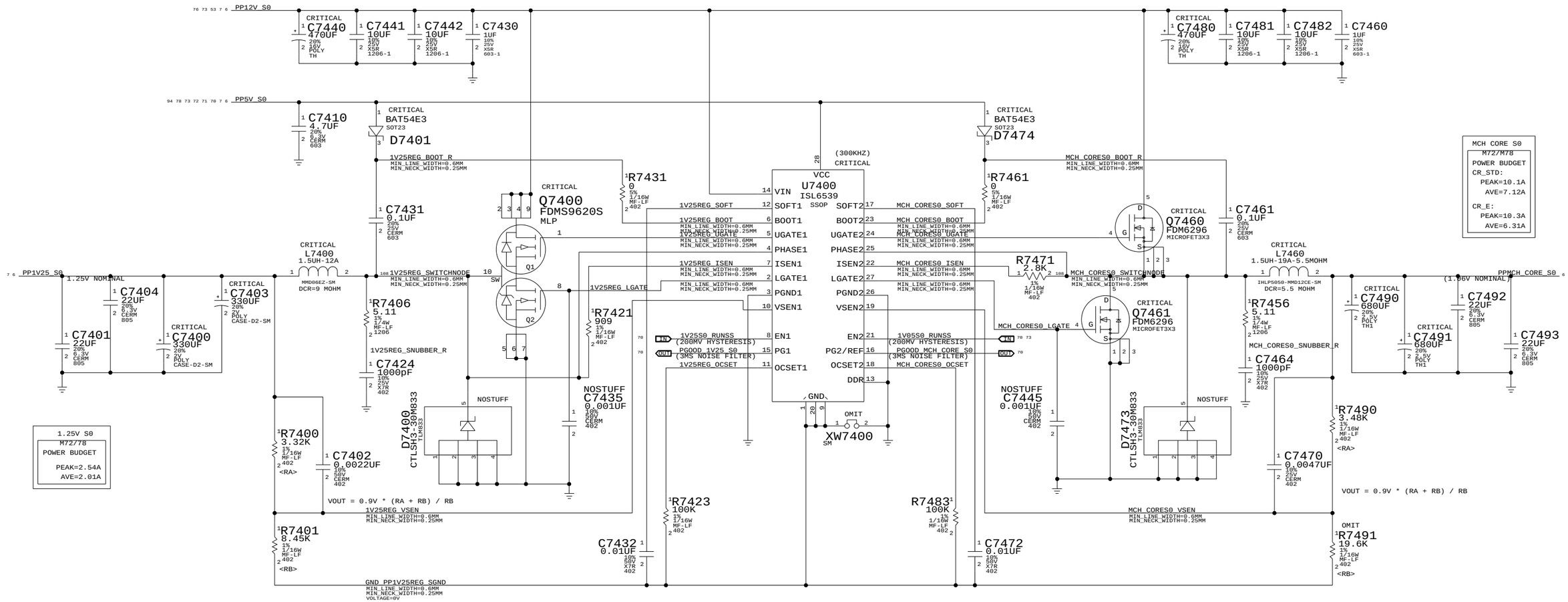
1.5V / 1.05V SUPPLIES

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 73 OF 118	

1.25V S0 & MCH CORE RAILS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0342	1	RES,MTL FILM,1/16W,19.6K,1,0402,SMD,LF	R7491		CR_STD
114S0309	1	RES,MTL FILM,1/16W,8.66K,1,0402,SMD,LF	R7491		CR_E

1.25V / MCH CORE SUPPLIES

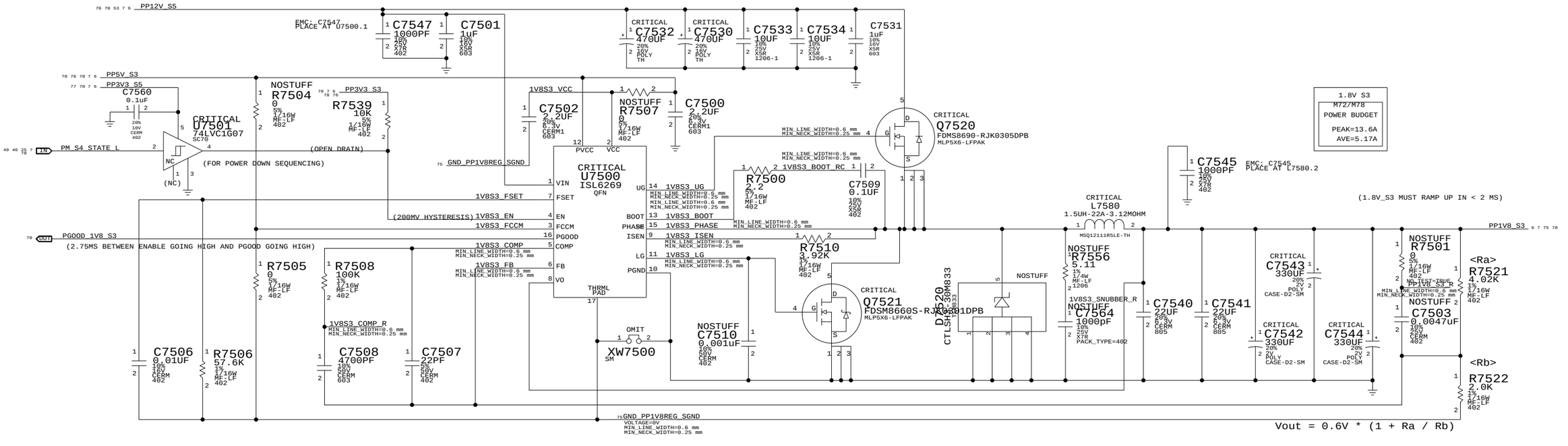
SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

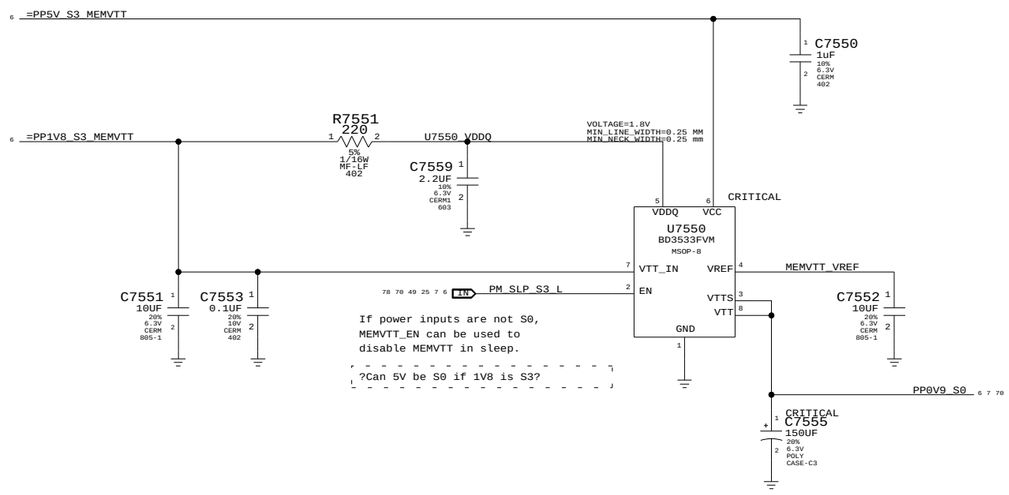
SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE SHT 74 OF 118

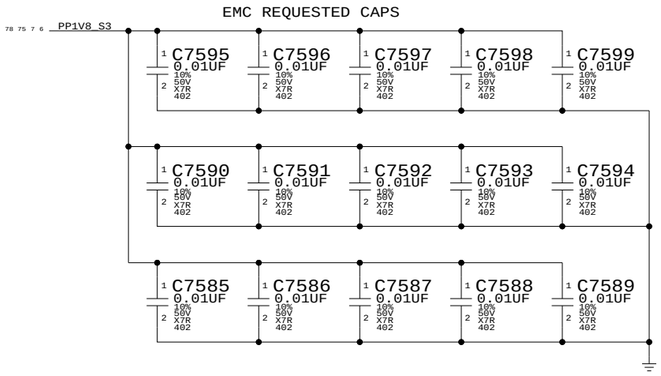
1.8V S3 / MEM VTT RAILS



DDR2 Vtt Regulator



EMC REQUESTED CAPS



1.8V S3 /0.9V S0 SUPPLIES

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 75 OF 118	

5V S5 & 3.3V S3 RAILS

(DUAL PACKAGE: SUPPLY PINS CONNECTED ON BOTTOM OF PAGE)

Vout = 0.8V * (1 + Rc / Rd)

(3.34V NOMINAL)

(5.0V NOMINAL)

(CHANGE FCB IF WE DON'T MEET E*)

(REPEATED FOR EASE OF ROUTING)

(HYSTERESIS)
(R7631: 71.5K; R7630: 40.2K; 300MV HYSTERESIS)

3.3V S3
M72778
POWER BUDGET
PEAK=6.06A
AVE=3.06A

5V S5
M72/M78
POWER BUDGET
M72 PEAK=12.0A
M72 AVE=6.83A
M78 PEAK=8.91A
M78 AVE=5.33A

5V S5 / 3.3V S3 SUPPLIES

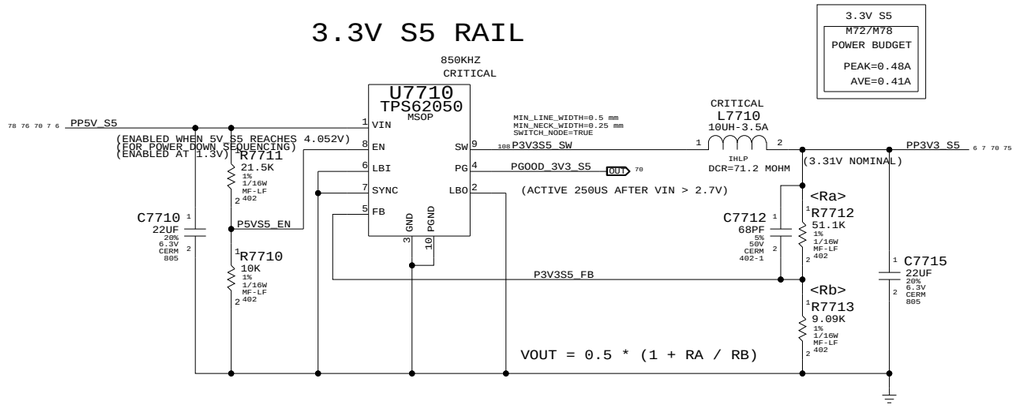
SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

NOTICE OF PROPRIETARY PROPERTY

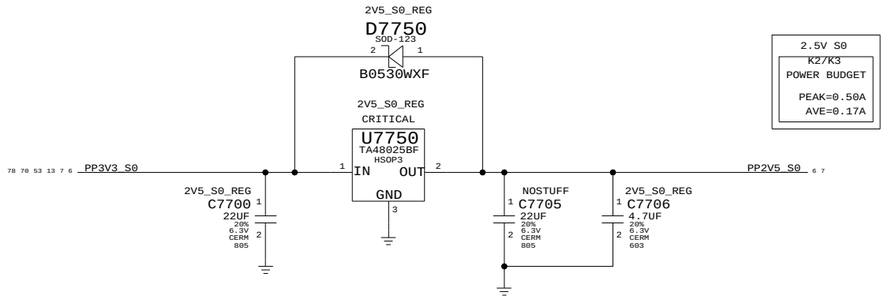
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 76 OF 118	

3.3V S5 RAIL



2.5V S0 RAIL (LDO)



State	Manageability	SMC_PM_G2_ENABLE	PM_S4_STATE_L	PM_SLP_S3_L	PM_SLP_S4_L	PM_SLP_M_L
Run (S0/M0)	N/A	1	1	1	1	1
Sleep (S3/M1)	On	1	1	0	1	1
Soft-Off (S5/M1)	On	1	0	0	1	1
Sleep (S3/M-Off)	Off	1	1	0	1	0
Soft-Off (S5/M-Off)	Off	1	0	0	0	0
Battery Off (G3Hot)	N/A	0	0	0	0	0

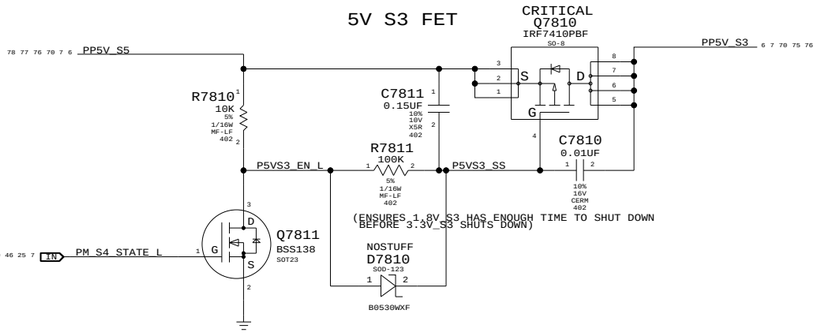
3.3V / 2.5V POWER SUPPLIES

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

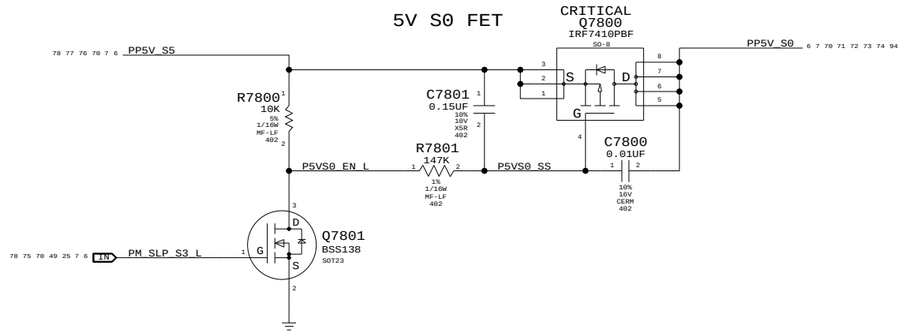
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 77 OF 118	

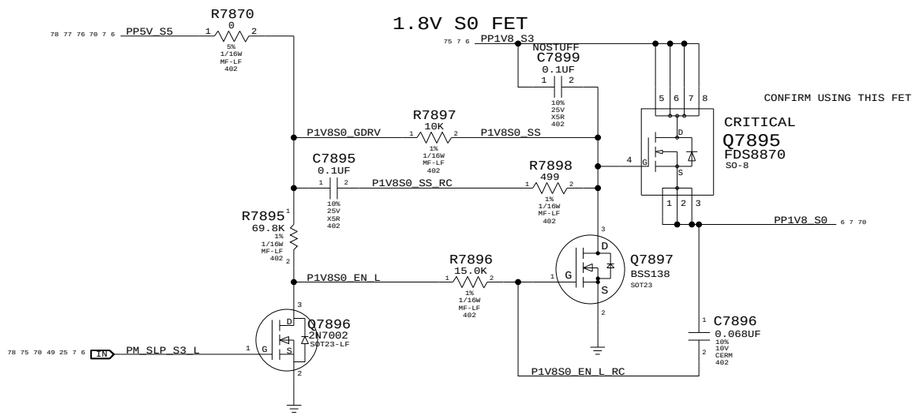
5V S3 FET



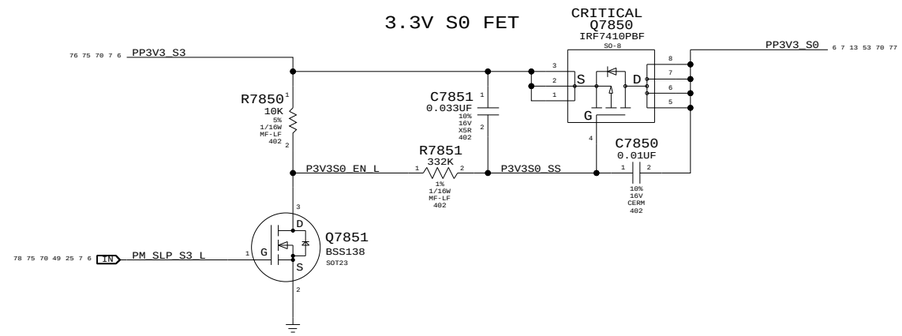
5V S0 FET



1.8V S0 FET



3.3V S0 FET



	I	Rds(on)	Vgs +/-
IRF7410	13A	7mOHM	8V
IRF7413	9.6A	18mOHM	20V
FDS4435	8.8A	35mOHM	25V
IRF7406	5.8A	70mOHM	20V
IRF6402	3.7A	65mOHM	12V
SI2302	1.6A	115mOHM	8V

S3 & S0 FETs

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 78 OF 118	

Page Notes

Power aliases required by this page:
- =PP12V_S0_MXM
- =PP5V_S0_MXM
- =PP1V8_S0_MXM

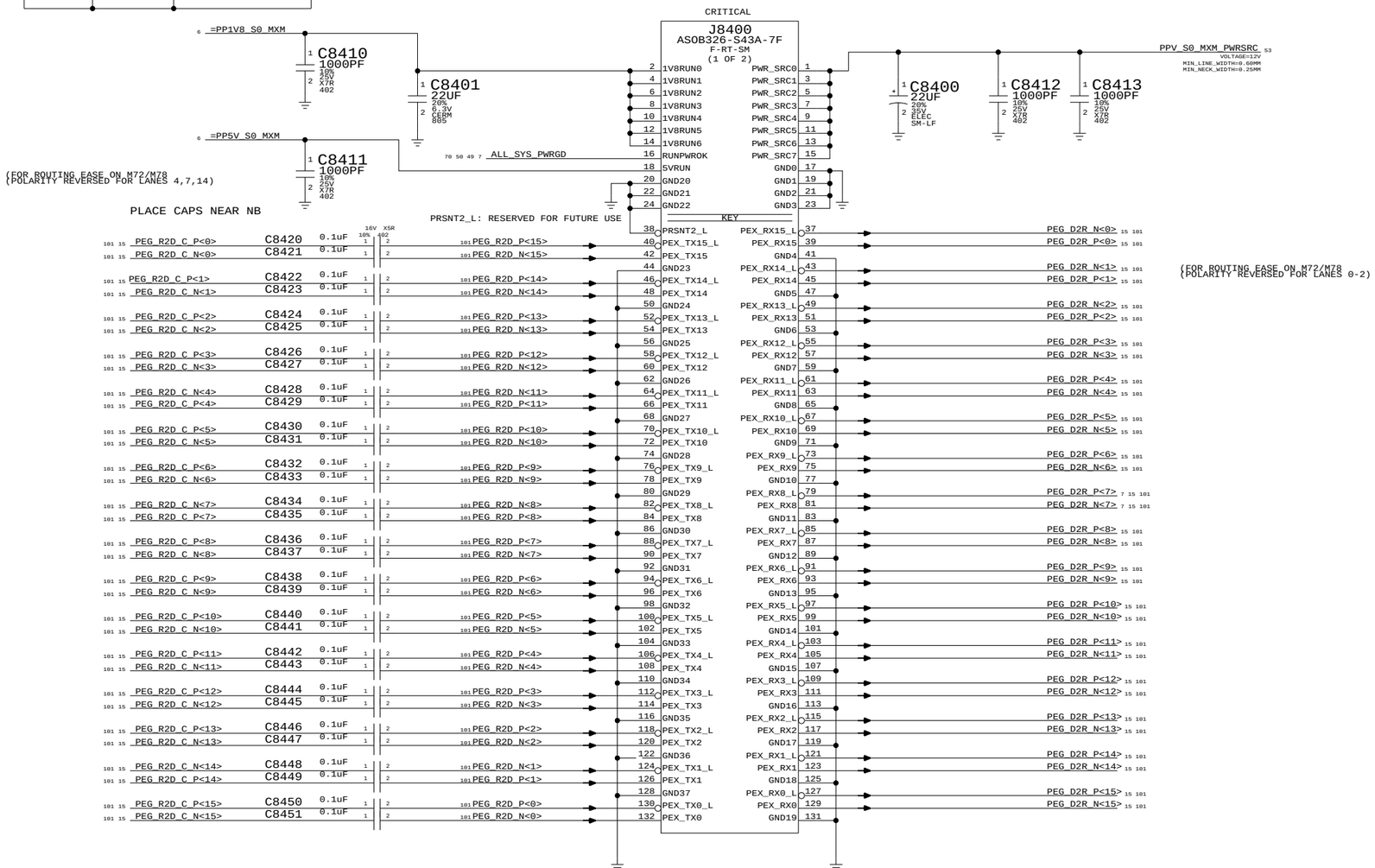
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Note: PCI-E Lanes are reversed to untangle routes
Need to stuff config strap using BOM option NBCFG_PEG_REVERSE
Polarity is also inverted (Tx+ goes to Rx-) to untangle routes

MXM SPEC POWER REQUIREMENTS
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT



MXM PCI-E & PWR

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE SHT 84 OF 118

Page Notes

Power aliases required by this page:
- =PP3V3_S0_MXM
- =PP2V5_S0_MXM

Signal aliases required by this page:
- =SMB_GPU_THRM_DATA
- =SMB_GPU_THRM_CLK

BOM options provided by this page:
24_INCH_LCD

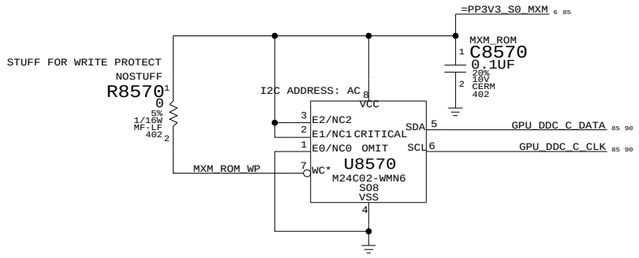
MXM SPEC POWER REQUIREMENTS

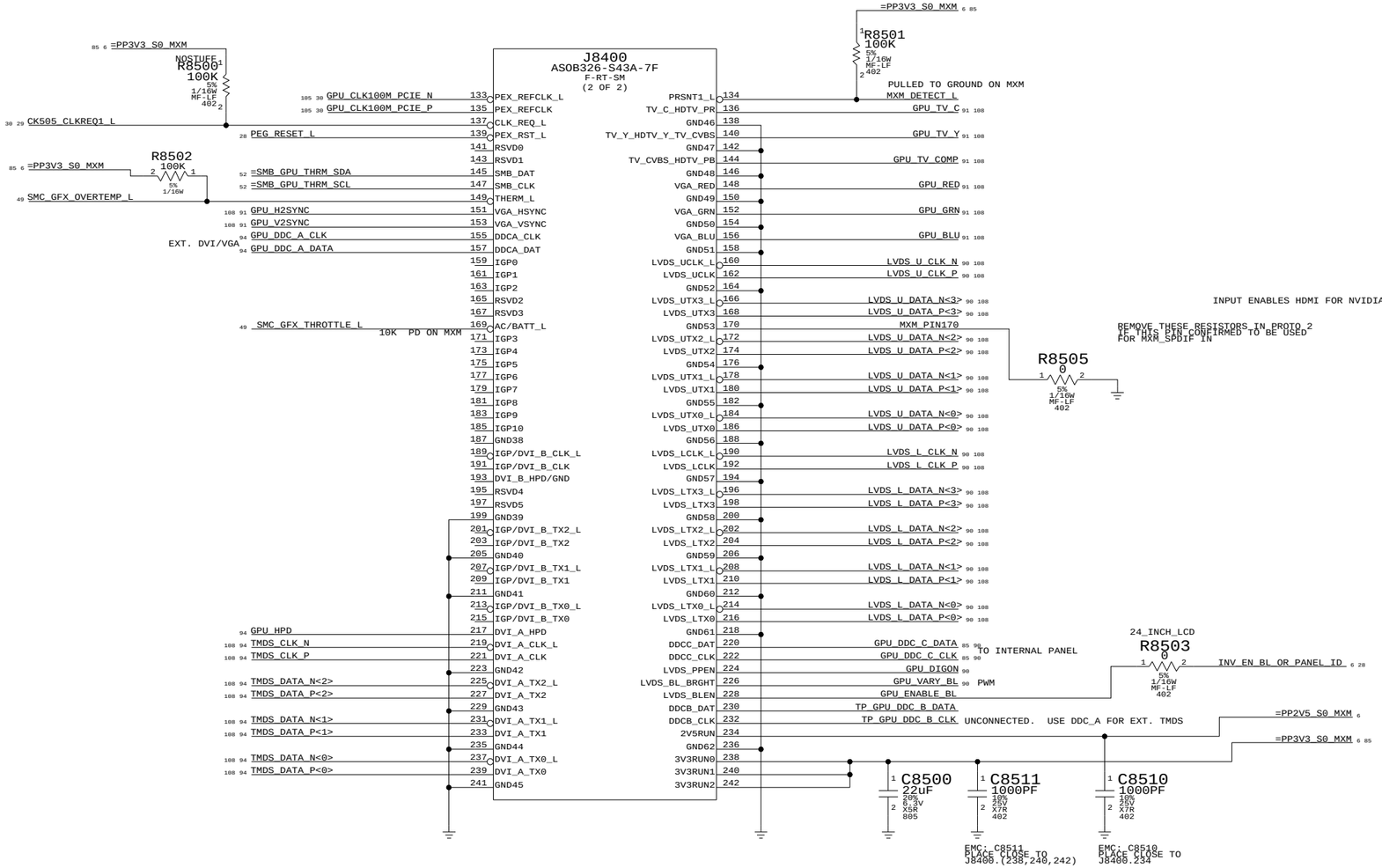
(NOT NECESSARILY THE SAME FOR EVERY MODULE)

VOLTAGE	CURRENT	POWER
3V3	1.5 A	4.95 W
5V	0.5 A	2.5 W
2V5	0.5 A	1.25 W
1V8	3.5 A	6.3 W
PWR (12V)	UP TO 4 A	PLATFORM DEPENDENT

MXM SYSTEM INFORMATION ROM

PLACE CLOSE TO J8400





MXM I/O

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE: NONE	SHT 85 OF 118	

Page Notes

Power aliases required by this page:
- =PPV_S0_LCD_24INCH
- =PPV_S0_LCD_20INCH
- =PP3V3_S0_VIDEO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
20_INCH_LCD, 24_INCH_LCD

94 91 6 =PP3V3_S0_VIDEO — I20 — =PP3V3_DDC_LCD 90

LCD (LVDS) INTERFACE

24_INCH_LCD
R9002 0 5% 1/8W MF-LF 805
6 =PPV_S0_LCD_24INCH

20_INCH_LCD
R9003 0 5% 1/8W MF-LF 805
6 =PPV_S0_LCD_20INCH

PANEL POWER SEQUENCING

PPV_S0_LCD
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

NOSTUFF
R9090 0 5% 1/8W MF-LF 805

C9000 0.1UF 10% 50V X7R 603-1

PLACE NEAR J9002

R9000 100K 5% 1/10W MF-LF 402

R9001 29.4K 1% 1/10W MF-LF 402

CRITICAL
Q9000 SI3443DV TSOP-LF

LCD_PWREN_L_RC

PPV_LCD_SW
VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

L9000 FERR-250-OHM SM

VOLTAGE=12V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

PPV_LCD_CONN 6 90
5V FOR 20 INCH LCD
12V FOR 24 INCH LCD

C9020 10UF 10% 16V X5R-CERM 1210

C9001 0.001uF 20% 50V CERM 402

LCD_PWREN_DIV

OMIT
R9099 100K 5% 1/10W MF-LF 402

LCD_PWREN_L

Q9001 2N7002 SOT23-LF

85 GPU_DIGON

R9070 100K 5% 1/10W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S0114	1	RES,100K,5%,0402	R9099		24_INCH_LCD
116S0004	1	RES,0,5%,0402	R9099		20_INCH_LCD

CRITICAL
SDF9000
STDOFF-4.00D4.6H-1.35-2.4-TH

516S0241
CRITICAL
J9002
53307-3052
F-ST-SM

108 85 LVDS_U_DATA_N<0>	1	2	LVDS_U_DATA_P<0> 85 108
108 85 LVDS_U_DATA_N<1>	3	4	LVDS_U_DATA_P<1> 85 108
108 85 LVDS_U_DATA_N<2>	5	6	LVDS_U_DATA_P<2> 85 108
	7	8	LVDS_U_CLK_N 85 108
108 85 LVDS_U_CLK_P	9	10	LVDS_U_DATA_N<3> 85 108
108 85 LVDS_U_DATA_P<3>	11	12	LVDS_L_DATA_N<0> 85 108
108 85 LVDS_L_DATA_P<0>	13	14	
108 85 LVDS_L_DATA_N<1>	15	16	LVDS_L_DATA_P<1> 85 108
	17	18	LVDS_L_DATA_N<2> 85 108
108 85 LVDS_L_DATA_P<2>	19	20	LVDS_L_CLK_N 85 108
108 85 LVDS_L_CLK_P	21	22	LVDS_L_DATA_N<3> 85 108
108 85 LVDS_L_DATA_P<3>	23	24	
85 GPU_DDC_C_CLK	25	26	GPU_DDC_C_DATA 85
	27	28	
	29	30	

90 =PP3V3_DDC_LCD
90 6 PPV_LCD_CONN
PPV_LCD_CONN 6 90

Panel has 4.7K DDC pull-ups
MXM also has 2.2K pull-ups

C9010 0.001uF 20% 50V CERM 402

CRITICAL
SDF9001
STDOFF-4.00D4.6H-1.35-2.4-TH

INVERTER INTERFACE

INVERTER CONNECTOR INCORPORATED INTO AC/DC CONNECTOR

85 GPU_VARY_BL
R9075 47 5% 1/10W MF-LF 402
LCD_PWM 6

NOSTUFF
R9074 10K 5% 1/10W MF-LF 402

INTERNAL DISPLAY CONNS

SYNC_MASTER=K2_MASTER
SYNC_DATE=N/A

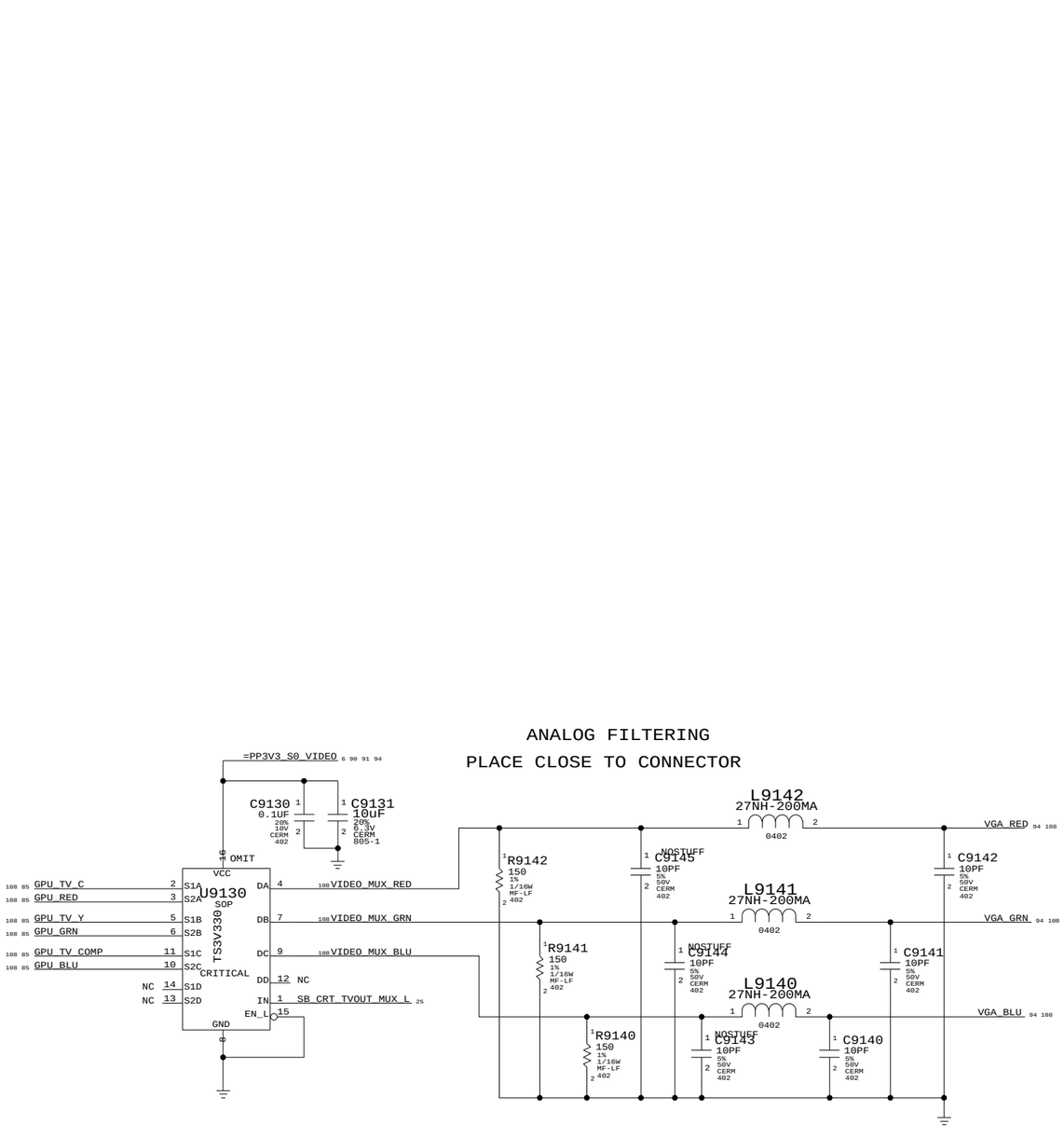
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE: NONE
SHT 90 OF 118

ANALOG FILTERING

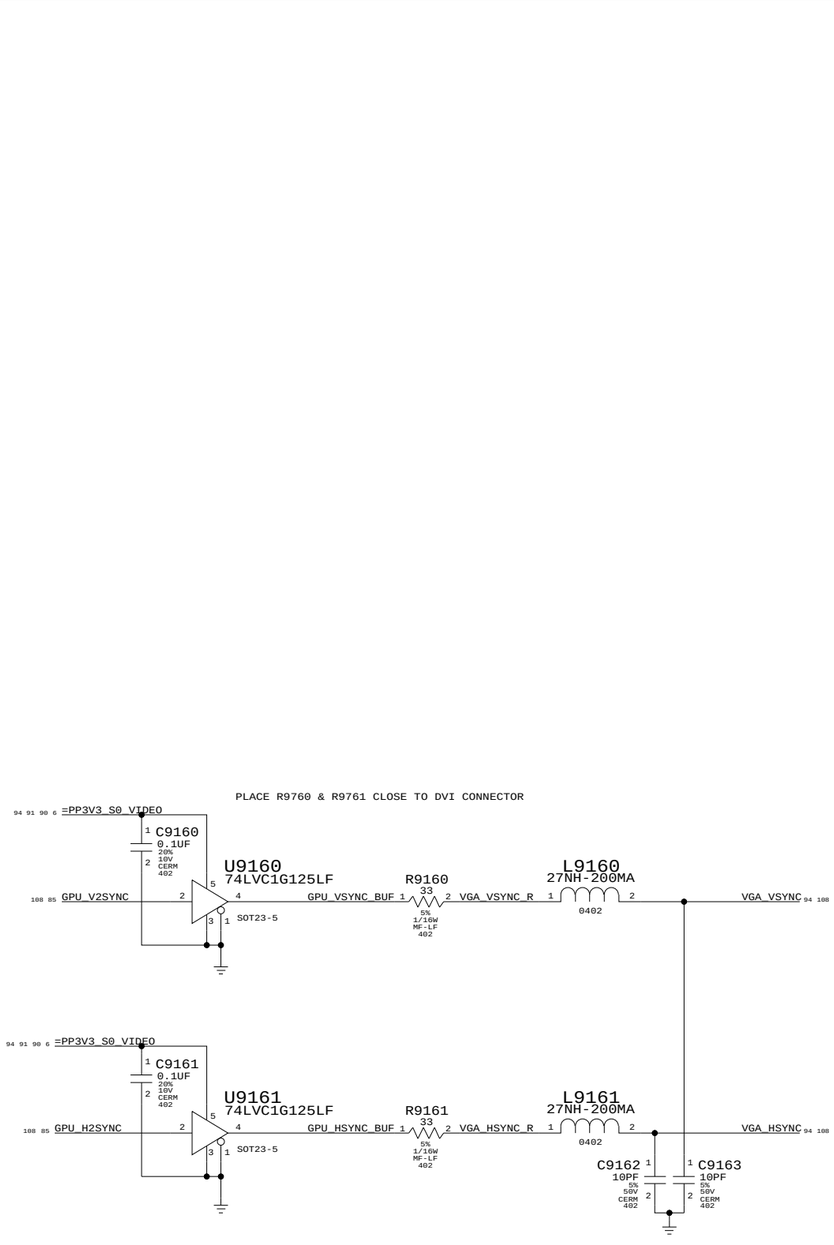
PLACE CLOSE TO CONNECTOR



VIDEO_MUX_SEL	OUT
1	CRT
0	TV

PLACE U9120 NEAR GMCH

PLACE R9760 & R9761 CLOSE TO DVI CONNECTOR



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S1700	1	QUAD SPDT HIGH-BANDWITDH VIDEO SWITCH,LOW ON-RES	U9130	CRITICAL	

Analog Video Support

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

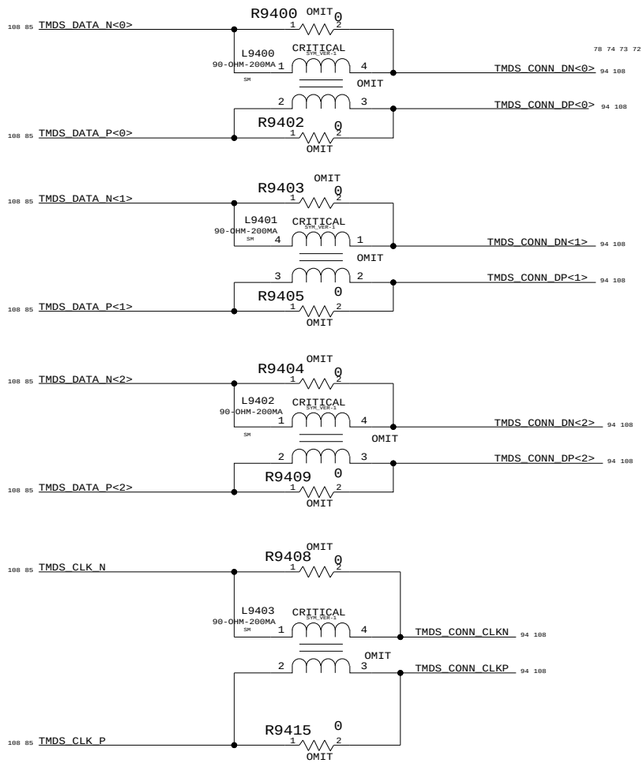
APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A
SCALE NONE	SHT 91 OF 118	

DVI INTERFACE

TMDS TERMINATION, IF ANY, IS ON MXM CARD

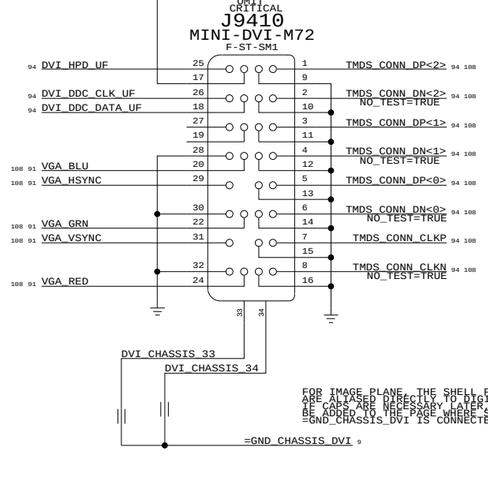
PLACE FILTER CLOSE TO MINI-DVI CONNECTOR



DVI DDC CURRENT LIMIT

(55mA requirement per DVI spec)

DON'T USE M51 SPECIFIC: 514S0129
APPLE PN: 514S0204

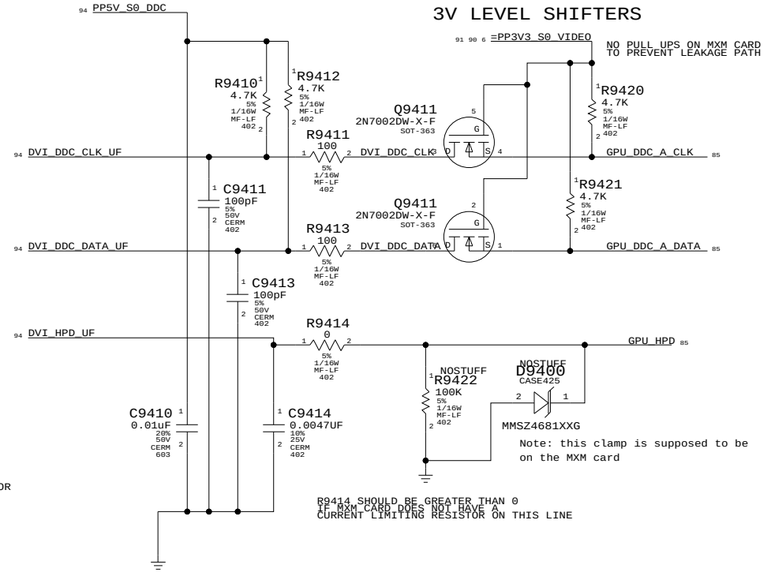


FOR IMAGE PLANE, THE SHELL PINS OF THE CONNECTOR ARE ALIASED DIRECTLY TO DIGITAL GROUND. IF CAPS ARE NECESSARY LATER, THEY SHOULD BE ADDED TO THE PAGE WHERE =SIGNAL =GND_CHASSIS_DVI IS CONNECTED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514S0204	1	CONN,RCPT,MINI_DVI,SMT,14 DGE,	J9410	CRITICAL	

PLACE CLOSE TO MINI-DVI CONNECTOR

3V LEVEL SHIFTERS



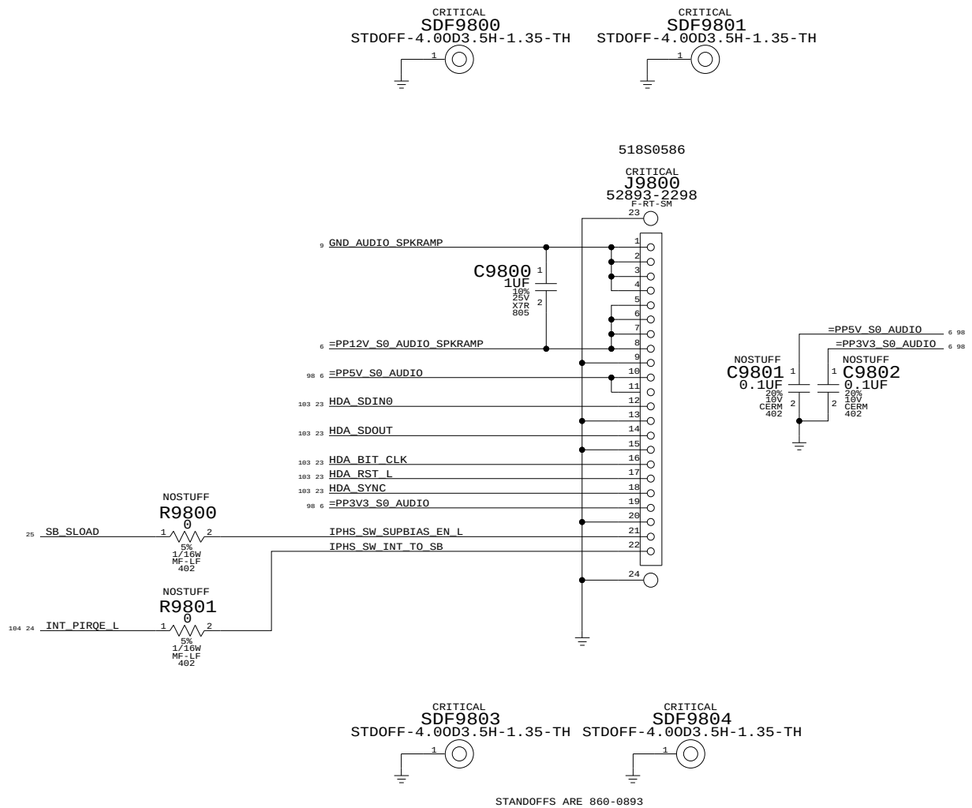
External Display Conns

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE	SHT	OF
NONE	94	118



STANDOFFS ARE 860-0893

MLB: AUDIO CONNECTOR

SYNC_MASTER=K2_MASTER SYNC_DATE=N/A

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE	SHT	OF
NONE	98	118

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_DSTB_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FSB_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	*	*	SPACING_0.2MM
FSB_ADSTB	*	*	SPACING_0.3MM
FSB_DATA	*	*	SPACING_0.2MM
FSB_DSTB	*	*	SPACING_0.3MM
FSB_COMMON	*	*	SPACING_0.2MM

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 1:1 and routed as differential pairs.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.2 & 4.3

CPU Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CPU_55S	*	55_OHM_SE
CPU_27P4S	*	27P4_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_2TO1	*	*	SPACING_0.2MM
CPU_COMP	*	*	SPACING_0.6MM
CPU_GTLREF	*	*	SPACING_0.6MM
CPU_ITP	*	*	SPACING_0.2MM
CPU_VCCSENSE	*	*	SPACING_0.6MM

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target differential impedance.

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Santa Rosa Platform DG, Rev 0.9 (#20517), Sections 4.4 & 5.8.2.4

CPU / FSB Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_ADS_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BNR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_BPRI_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_BREQ0_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DBSY_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DEFER_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_DRDY_L	10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HIT_L	7 10 14
FSB_COMMON_PP	FSB_55S	FSB_COMMON	FSB_HITM_L	7 10 14
FSB_COMMON_2PP	FSB_55S	FSB_COMMON	FSB_LOCK_L	7 10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	10 14
FSB_COMMON	FSB_55S	FSB_COMMON	FSB_TRDY_L	10 14
FSB_CPURST_L	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 10 13 14
FSB_DATA_GROUP0	FSB_55S	FSB_DATA	FSB_D_L<15..1>	10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_D_L<0>	7 10 14
FSB_DATA_GROUP0_PP	FSB_55S	FSB_DATA	FSB_DINV_L<0>	7 10 14
FSB_DSTB0	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<0>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<0>	7 10 14
FSB_DATA_GROUP1	FSB_55S	FSB_DATA	FSB_D_L<31..17>	10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_D_L<16>	7 10 14
FSB_DATA_GROUP1_PP	FSB_55S	FSB_DATA	FSB_DINV_L<1>	7 10 14
FSB_DSTB1	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<1>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<1>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<47..42>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_D_L<41>	7 10 14
FSB_DATA_GROUP2	FSB_55S	FSB_DATA	FSB_D_L<40..32>	10 14
FSB_DATA_GROUP2_PP	FSB_55S	FSB_DATA	FSB_DINV_L<2>	7 10 14
FSB_DSTB2	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<2>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<2>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<63..60>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_D_L<59>	7 10 14
FSB_DATA_GROUP3	FSB_55S	FSB_DATA	FSB_D_L<58..48>	10 14
FSB_DATA_GROUP3_PP	FSB_55S	FSB_DATA	FSB_DINV_L<3>	7 10 14
FSB_DSTB3	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_P<3>	7 10 14
	FSB_DSTB_55S	FSB_DSTB	FSB_DSTB_L_N<3>	7 10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<16..7>	10 14
FSB_ADDR_GROUP0	FSB_55S	FSB_ADDR	FSB_A_L<5..3>	10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_A_L<6>	7 10 14
FSB_ADDR_GROUP0_PP	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	7 10 14
FSB_ADSTB0	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<0>	7 10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<35..28>	10 14
FSB_ADDR_GROUP1	FSB_55S	FSB_ADDR	FSB_A_L<26..17>	10 14
FSB_ADDR_GROUP1_PP	FSB_55S	FSB_ADDR	FSB_A_L<27>	7 10 14
FSB_ADSTB1	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<1>	7 10 14
CPU_IERR_L	CPU_55S		CPU_IERR_L	10
CPU_FERR_L	CPU_55S		CPU_FERR_L	10 23
CPU_PROCHOT_L	CPU_55S	CPU_2TO1	CPU_PROCHOT_L	10 50 55
CPU_PWRGD	CPU_55S		CPU_PWRGD	7 10 13 23
CPU_FROM_SB_PP	CPU_55S		CPU_INTR	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_NMI	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_A20M_L	7 10 23
CPU_FROM_SB	CPU_55S		CPU_DPSLP_L	10 23
CPU_FROM_SB_PP	CPU_55S		CPU_IGNNE_L	7 10 23
CPU_INIT_L	CPU_55S		CPU_INIT_L	7 10 23 51
CPU_FROM_SB_PP	CPU_55S		CPU_SMI_L	7 10 23
CPU_FROM_SB_PP	CPU_55S		CPU_STPCLK_L	7 10 23
PM_THRMTRIP_L	CPU_55S	CPU_2TO1	PM_THRMTRIP_L	10 16 23 50
FSB_CPUSLP_L	CPU_55S		FSB_CPUSLP_L	10 14
PM_DPRSLPVR	CPU_55S	CPU_2TO1	PM_DPRSLPVR	16 25 71
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	71
CPU_BSEL0	CPU_55S	CPU_2TO1	CPU_BSEL<0>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<0>	13 16 30
CPU_BSEL1	CPU_55S	CPU_2TO1	CPU_BSEL<1>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<1>	13 16 30
CPU_BSEL2	CPU_55S	CPU_2TO1	CPU_BSEL<2>	10 30
	CPU_55S	CPU_2TO1	NB_BSEL<2>	13 16 30
CPU_DPRSTP_L	CPU_55S	CPU_2TO1	CPU_DPRSTP_L	10 16 23 71
CPU_GTLREF	CPU_55S	CPU_GTLREF	CPU_GTLREF	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<3>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<2>	10
CPU_COMP	CPU_55S	CPU_COMP	CPU_COMP<1>	10
CPU_COMP	CPU_27P4S	CPU_COMP	CPU_COMP<0>	10
XDP_TDI	CPU_55S	CPU_ITP	XDP_TDI	10 13
XDP_TDO	CPU_55S	CPU_ITP	XDP_TDO	10 13
XDP_TMS	CPU_55S	CPU_ITP	XDP_TMS	10 13
XDP_TCK	CPU_55S	CPU_ITP	XDP_TCK	10 13
XDP_TRST_L	CPU_55S	CPU_ITP	XDP_TRST_L	10 13
XDP_BPM_L	CPU_55S	CPU_ITP	XDP_BPM_L<4..0>	10 13
XDP_BPM_L5	CPU_55S	CPU_ITP	XDP_BPM_L<5>	10 13
	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 105
	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 105
(FSB_CPURST_L)	CPU_55S	CPU_ITP	ITP_CPURST_L	
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	11 12
	CPU_55S	CPU_2TO1	IMVP6_VID<6..0>	12 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	11 71
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	11 71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	71
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	71

CPU/FSB Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

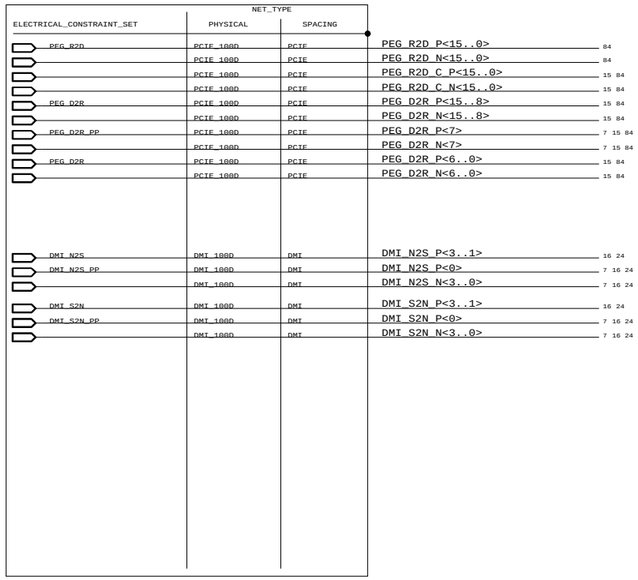
SCALE NONE SHT 100 OF 118

PCI-Express / DMI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCIE_100D	*	100_OHM_DIFF
DMI_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE	*	*	SPACING_0.5MM
DMI	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 7.2, 9.2 & 10.5



Video Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS_100D	*	100_OHM_DIFF
CRT_55S	*	55_OHM_SE
CRT_50S	*	50_OHM_SE
TMDS_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET	
LVDS	*	*	SPACING_0.5MM	
CRT	*	*	SPACING_0.6MM	DG Says 40 mil spacing minimum
CRT	CRT	*	SPACING_0.5MM	
TVDAC				DG Says 30 mil spacing minimum
CRT_SYNC	*	*	SPACING_0.6MM	
CRT_SYNC	CRT_SYNC	*	SPACING_0.5MM	DG Says 40 mil spacing minimum
TMDS	*	*	SPACING_0.5MM	

LVDS signals are 100-ohm +/- 20% differential impedence.
CRT & TVDAC signal single-ended impedence varies by location:
- 37.5-ohm +/- 15% from GMCH to first termination resistor.
- 50-ohm +/- 15% from first to second termination resistor.
- 55-ohm +/- 15% from second termination resistor to connector.
CRT_HSYNC/CRT_VSYNC signals are 55-ohm +/- 15% single-ended impedence.

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 8.1 - 8.3.

NB Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

SCALE NONE SHT 101 OF 118

DDR2 Memory Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
MEM_45S	*	45_OHM_SE
MEM_55S	*	55_OHM_SE
MEM_70D	*	70_OHM_DIFF
MEM_85D	*	85_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	SPACING_0.6MM
MEM_CMD	*	*	SPACING_0.15MM
MEM_CTRL	*	*	SPACING_0.6MM
MEM_DATA	*	*	SPACING_0.6MM
MEM_DQS	*	*	SPACING_0.6MM
MEM_CLK	MEM_CLK	*	SPACING_0.4MM
MEM_CLK	MEM_CTRL	*	SPACING_0.4MM
MEM_CLK	MEM_CMD	*	SPACING_0.4MM
MEM_CLK	MEM_DATA	*	SPACING_0.4MM
MEM_CLK	MEM_DQS	*	SPACING_0.4MM
MEM_CTRL	MEM_CTRL	*	SPACING_0.2MM
MEM_CTRL	MEM_CMD	*	SPACING_0.3MM
MEM_CTRL	MEM_DATA	*	SPACING_0.3MM
MEM_CTRL	MEM_DQS	*	SPACING_0.3MM
MEM_CMD	MEM_CMD	*	SPACING_0.15MM
MEM_CMD	MEM_DATA	*	SPACING_0.3MM
MEM_CMD	MEM_DQS	*	SPACING_0.3MM
MEM_DATA	MEM_DATA	*	SPACING_0.15MM
MEM_DATA	MEM_DQS	*	SPACING_0.3MM
MEM_DQS	MEM_DQS	*	SPACING_0.3MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 6.2

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<1..0>	16 31
	MEM_70D	MEM_CLK	MEM_CLK_N<1..0>	16 31
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<1..0>	16 31 33
MEM_A_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<1..0>	16 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_A<14..0>	16 17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_BS<2..0>	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_RAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_CAS_L	17 31 33
MEM_A_CMD	MEM_55S	MEM_CMD	MEM_A_WE_L	17 31 33
MEM_A_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_A_DQ<6..0>	17 31
MEM_A_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_A_DQ<7>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<13..8>	17 31
MEM_A_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_A_DQ<14>	7 17 31
MEM_A_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_A_DQ<15>	17 31
MEM_A_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_A_DQ<16>	7 17 31
MEM_A_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_A_DQ<23..17>	17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<24>	17 31
MEM_A_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_A_DQ<25>	7 17 31
MEM_A_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_A_DQ<31..26>	17 31
MEM_A_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_A_DQ<38..32>	17 31
MEM_A_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_A_DQ<39>	7 17 31
MEM_A_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_A_DQ<46..40>	17 31
MEM_A_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_A_DQ<47>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<53..48>	17 31
MEM_A_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_A_DQ<54>	7 17 31
MEM_A_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_A_DQ<55>	17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<58..56>	17 31
MEM_A_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_A_DQ<59>	7 17 31
MEM_A_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_A_DQ<63..60>	17 31
MEM_A_DM0	MEM_55S	MEM_DATA	MEM_A_DM<0>	17 31
MEM_A_DM1	MEM_55S	MEM_DATA	MEM_A_DM<1>	17 31
MEM_A_DM2	MEM_55S	MEM_DATA	MEM_A_DM<2>	17 31
MEM_A_DM3	MEM_55S	MEM_DATA	MEM_A_DM<3>	17 31
MEM_A_DM4	MEM_55S	MEM_DATA	MEM_A_DM<4>	17 31
MEM_A_DM5	MEM_55S	MEM_DATA	MEM_A_DM<5>	17 31
MEM_A_DM6	MEM_55S	MEM_DATA	MEM_A_DM<6>	17 31
MEM_A_DM7	MEM_55S	MEM_DATA	MEM_A_DM<7>	17 31
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	7 17 31
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	7 17 31
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	7 17 31
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	7 17 31
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	7 17 31
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	7 17 31
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	7 17 31
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	7 17 31
	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	7 17 31

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_B_CLK	MEM_70D	MEM_CLK	MEM_CLK_P<4..3>	16 32
	MEM_70D	MEM_CLK	MEM_CLK_N<4..3>	16 32
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CKE<4..3>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_CS_L<3..2>	16 32 33
MEM_B_CNTL	MEM_45S	MEM_CTRL	MEM_ODT<3..2>	16 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_A<14..0>	16 17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_BS<2..0>	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_RAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_CAS_L	17 32 33
MEM_B_CMD	MEM_55S	MEM_CMD	MEM_B_WE_L	17 32 33
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<5..0>	17 32
MEM_B_DQ_BYTE0_PP	MEM_55S	MEM_DATA	MEM_B_DQ<6>	7 17 32
MEM_B_DQ_BYTE0	MEM_55S	MEM_DATA	MEM_B_DQ<7>	17 32
MEM_B_DQ_BYTE1_PP	MEM_55S	MEM_DATA	MEM_B_DQ<8>	7 17 32
MEM_B_DQ_BYTE1	MEM_55S	MEM_DATA	MEM_B_DQ<15..9>	17 32
MEM_B_DQ_BYTE2	MEM_55S	MEM_DATA	MEM_B_DQ<22..16>	17 32
MEM_B_DQ_BYTE2_PP	MEM_55S	MEM_DATA	MEM_B_DQ<23>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<24>	17 32
MEM_B_DQ_BYTE3_PP	MEM_55S	MEM_DATA	MEM_B_DQ<25>	7 17 32
MEM_B_DQ_BYTE3	MEM_55S	MEM_DATA	MEM_B_DQ<31..26>	17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<37..32>	17 32
MEM_B_DQ_BYTE4_PP	MEM_55S	MEM_DATA	MEM_B_DQ<38>	7 17 32
MEM_B_DQ_BYTE4	MEM_55S	MEM_DATA	MEM_B_DQ<39>	17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<43..40>	17 32
MEM_B_DQ_BYTE5_PP	MEM_55S	MEM_DATA	MEM_B_DQ<44>	7 17 32
MEM_B_DQ_BYTE5	MEM_55S	MEM_DATA	MEM_B_DQ<47..45>	17 32
MEM_B_DQ_BYTE6_PP	MEM_55S	MEM_DATA	MEM_B_DQ<48>	7 17 32
MEM_B_DQ_BYTE6	MEM_55S	MEM_DATA	MEM_B_DQ<55..49>	17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<61..56>	17 32
MEM_B_DQ_BYTE7_PP	MEM_55S	MEM_DATA	MEM_B_DQ<62>	7 17 32
MEM_B_DQ_BYTE7	MEM_55S	MEM_DATA	MEM_B_DQ<63>	17 32
MEM_B_DM0	MEM_55S	MEM_DATA	MEM_B_DM<0>	17 32
MEM_B_DM1	MEM_55S	MEM_DATA	MEM_B_DM<1>	17 32
MEM_B_DM2	MEM_55S	MEM_DATA	MEM_B_DM<2>	17 32
MEM_B_DM3	MEM_55S	MEM_DATA	MEM_B_DM<3>	17 32
MEM_B_DM4	MEM_55S	MEM_DATA	MEM_B_DM<4>	17 32
MEM_B_DM5	MEM_55S	MEM_DATA	MEM_B_DM<5>	17 32
MEM_B_DM6	MEM_55S	MEM_DATA	MEM_B_DM<6>	17 32
MEM_B_DM7	MEM_55S	MEM_DATA	MEM_B_DM<7>	17 32
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	7 17 32
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	7 17 32
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	7 17 32
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	7 17 32
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	7 17 32
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	7 17 32
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	7 17 32
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	7 17 32
	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	7 17 32

Memory Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE INC.

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Disk Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
IDE_55S	*	55_OHM_SE
SATA_55S	*	55_OHM_SE
SATA_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
IDE	*	*	SPACING_0.18MM
SATA	*	*	SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.7 & 10.9

HD Audio Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
HDA_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
HDA	*	*	SPACING_0.18MM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
USB_60S	*	55_OHM_SE
USB_90D	*	90_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB	*	*	SPACING_0.5MM

DG SAYS MINIMUM SPACING 50 MILS FROM USB TO CLOCKS

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Section 10.13.2

Internal Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
SMB_55S	*	55_OHM_SE
SPI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SMB	*	*	SPACING_0.3MM
SPI	*	*	SPACING_0.18MM

SOURCE: Santa Platform DG, Rev 1.0 (#21112), Section 10.17

NET_TYPE ELECTRICAL_CONSTRAINT_SET	PHYSICAL	SPACING		
IDE_PDD	IDE_55S	IDE	IDE_PDD<15..10>	23 44
IDE_PDD_PP	IDE_55S	IDE	IDE_PDD<9>	7 23 44
IDE_PDD	IDE_55S	IDE	IDE_PDD<8..0>	23 44
IDE_PDA	IDE_55S	IDE	IDE_PDA<2..0>	23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS1_L	23 44
IDE_PDCS	IDE_55S	IDE	IDE_PDCS3_L	23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDIOW_L	23 44
IDE_PDIOR_L	IDE_55S	IDE	IDE_PDIOR_L	7 23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDACK_L	23 44
IDE_CNTL	IDE_55S	IDE	IDE_PDDREQ	23 44
IDE_PDIORDY	IDE_55S	IDE	IDE_PDIORDY	7 23 44
IDE_IRQ14	IDE_55S	IDE	IDE_IRQ14	23 44
IDE_RST_L	IDE_55S	IDE	ODD_RST_5VTOL_L	7 24 44
SATA_A_R2D	SATA_100D	SATA	SATA_A_R2D_C_P	23 45
	SATA_100D	SATA	SATA_A_R2D_C_N	23 45
	SATA_100D	SATA	SATA_A_R2D_P	45
	SATA_100D	SATA	SATA_A_R2D_N	45
SATA_A_D2R	SATA_100D	SATA	SATA_A_D2R_P	7 23 45
	SATA_100D	SATA	SATA_A_D2R_N	7 23 45
	SATA_100D	SATA	SATA_A_D2R_C_P	45
	SATA_100D	SATA	SATA_A_D2R_C_N	45
	SATA_100D	SATA	SATA_B_R2D_C_P	23 45
	SATA_100D	SATA	SATA_B_R2D_C_N	23 45
	SATA_100D	SATA	SATA_B_D2R_P	23 45
	SATA_100D	SATA	SATA_B_D2R_N	23 45
SATA_RBIAS	SATA_55S		SATA_RBIAS	45
HDA_BIT_CLK	HDA_55S	HDA	HDA_BIT_CLK	23 98
	HDA_55S	HDA	HDA_BIT_CLK_R	23
HDA_SYNC	HDA_55S	HDA	HDA_SYNC	23 98
	HDA_55S	HDA	HDA_SYNC_R	23
HDA_RST_L	HDA_55S	HDA	HDA_RST_L	23 98
	HDA_55S	HDA	HDA_RST_L_R	23
HDA_SDIN0	HDA_55S	HDA	HDA_SDIN0	23 98
	HDA_55S	HDA	HDA_SDIN_CODEC	
HDA_SDOUT	HDA_55S	HDA	HDA_SDOUT	23 98
	HDA_55S	HDA	HDA_SDOUT_R	23
USB_EXTA	USB_90D	USB	USB_EXTA_P	24 46
	USB_90D	USB	USB_EXTA_N	24 46
	USB_90D	USB	USB_EXTA_MUXED_P	
	USB_90D	USB	USB_EXTA_MUXED_N	
USB_MINI	USB_90D	USB	USB_MINI_P	24 34
	USB_90D	USB	USB_MINI_N	24 34
	USB_90D	USB	USB_EXTD_P	24 46
	USB_90D	USB	USB_EXTD_N	24 46
USB_CAMERA	USB_90D	USB	USB_CAMERA_P	7 24 47
	USB_90D	USB	USB_CAMERA_N	7 24 47
USB_BT	USB_90D	USB	USB_BT_P	7 24 47
	USB_90D	USB	USB_BT_N	7 24 47
	USB_90D	USB	USB_TPAD_P	24 47
	USB_90D	USB	USB_TPAD_N	24 47
USB_IR	USB_90D	USB	USB_IR_P	7 24 47
	USB_90D	USB	USB_IR_N	7 24 47
USB_EXTB	USB_90D	USB	USB_EXTB_P	24 46
	USB_90D	USB	USB_EXTB_N	24 46
	USB_90D	USB	USB_EXCARD_P	24 47
	USB_90D	USB	USB_EXCARD_N	24 47
USB_EXTC	USB_90D	USB	USB_EXTC_P	24 46
	USB_90D	USB	USB_EXTC_N	24 46
USB_RBIAS	USB_60S		USB_RBIAS	24
SMB_SB_SCL	SMB_55S	SMB	SMB_CLK	25 52
SMB_SB_SDA	SMB_55S	SMB	SMB_DATA	25 52
SMB_SB_ME_SCL	SMB_55S	SMB	SMB_ME_CLK	25 52
SMB_SB_ME_SDA	SMB_55S	SMB	SMB_ME_DATA	25 52
SPI_SCLK	SPI_55S	SPI	SPI_SCLK_R	7 24 61
	SPI_55S	SPI	SPI_SCLK	7 61
	SPI_55S	SPI	SPI_A_SCLK_R	
	SPI_55S	SPI	SPI_B_SCLK_R	
SPI_SI	SPI_55S	SPI	SPI_SI_R	24 61
	SPI_55S	SPI	SPI_SI	
	SPI_55S	SPI	SPI_A_SI_R	61
	SPI_55S	SPI	SPI_B_SI_R	
SPI_SO	SPI_55S	SPI	SPI_SO	7 24 61
	SPI_55S	SPI	SPI_A_SO_R	7 61
	SPI_55S	SPI	SPI_B_SO	
	SPI_55S	SPI	SPI_B_SO_R	
SPI_CE_L0	SPI_55S	SPI	SPI_CE_R_L<0>	24 61
	SPI_55S	SPI	SPI_CE_L<0>	7 61
SPI_CE_L1	SPI_55S	SPI	SPI_CE_R_L<1>	
	SPI_55S	SPI	SPI_CE_L<1>	

SB Constraints (1 of 2)

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE INC.

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PCI Bus Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
PCI_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCI	*	*	STANDARD

CHANGED TO 0.1MM SPACING AS THERE ARE NO PCI DEVICES

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.18.1 & 10.19

Controller Link (AMT) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLINK_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK	*	*	SPACING_0.18MM
CLINK_VREF	*	*	SPACING_0.3MM

PHYSICAL_RULE_SET	LAYER	ALLOW_ROUTE_ON_LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLINK_12MIL	*	=STANDARD	0.3 MM	0.125 MM	7.5 MM	=STANDARD	=STANDARD

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

Ethernet (Yukon) Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
ENET_100D	*	100_OHM_DIFF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	*	*	SPACING_0.5MM
ENET_MDI	ENET_MDI_TERM	*	SPACING_0.2MM

SOURCE: Based on Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 10.27.1.5-7, 10.29 & 10.30

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	PCI_55S	PCI	PCI_AD<18..0>	24 28
	PCI_55S	PCI	PCI_AD<19>	24 28
	PCI_55S	PCI	PCI_AD<20>	24 28
	PCI_55S	PCI	PCI_AD<31..21>	24 28
	PCI_55S	PCI	PCI_PAR	24 28
	PCI_55S	PCI	PCI_C_BE_L<3..0>	24 28
	PCI_55S	PCI	PCI_IRDY_L	24
	PCI_55S	PCI	PCI_DEVSEL_L	24
	PCI_55S	PCI	PCI_PERR_L	24
	PCI_55S	PCI	PCI_LOCK_L	24
	PCI_55S	PCI	PCI_SERR_L	7 24 28
	PCI_55S	PCI	PCI_STOP_L	24
	PCI_55S	PCI	PCI_TRDY_L	24
	PCI_55S	PCI	PCI_FRAME_L	24
	PCI_55S	PCI	PCI_FW_REQ_L	24
	PCI_55S	PCI	PCI_FW_GNT_L	24
	PCI_55S	PCI	PCI_REQ1_L	7 24
	PCI_55S	PCI	PCI_GNT1_L	
	PCI_55S	PCI	PCI_REQ2_L	7 24
	PCI_55S	PCI	PCI_GNT2_L	
INT_PIRQA_L	PCI_55S	PCI	INT_PIRQA_L	24
INT_PIRQB_L	PCI_55S	PCI	INT_PIRQB_L	24
INT_PIRQC_L	PCI_55S	PCI	INT_PIRQC_L	24
INT_PIRQD_L	PCI_55S	PCI	INT_PIRQD_L	24
INT_PIRQE_L	PCI_55S	PCI	INT_PIRQE_L	24 98
INT_PIRQF_L	PCI_55S	PCI	INT_PIRQF_L	24
PCIE_A_R2D	PCIE_100D	PCIE	PCIE_MINI_R2D_C_P	24 34
	PCIE_100D	PCIE	PCIE_MINI_R2D_C_N	24 34
PCIE_A_D2R	PCIE_100D	PCIE	PCIE_MINI_D2R_P	7 24 34
	PCIE_100D	PCIE	PCIE_MINI_D2R_N	7 24 34
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_ENET_R2D_C_P	24 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_C_N	24 37
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_ENET_D2R_P	7 24 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_N	7 24 37
PCIE_B_R2D	PCIE_100D	PCIE	PCIE_FW_R2D_C_P	40 42
	PCIE_100D	PCIE	PCIE_FW_R2D_C_N	40 42
PCIE_B_D2R	PCIE_100D	PCIE	PCIE_FW_D2R_P	7 40 42
	PCIE_100D	PCIE	PCIE_FW_D2R_N	7 40 42
GLAN_COMP			GLAN_COMP	23
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_CLK	7 16 25
CLINK_NB	CLINK_55S	CLINK	CLINK_NB_DATA	7 16 25
CLINK_NB_RESET_L	CLINK_55S	CLINK	CLINK_NB_RESET_L	16 25
NB_CLINK_VREF	CLINK_12MIL	CLINK_VREF	NB_CLINK_VREF	16
SB_CLINK_VREF0	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF0	25
SB_CLINK_VREF1	CLINK_12MIL	CLINK_VREF	SB_CLINK_VREF1	25
1140		PWR	PP1V9_ENET_PHY_AVDD	37
1142		ENET_MDI_TERM	ENET_MDI0	37
1143		ENET_MDI_TERM	ENET_MDI1	37
1145		ENET_MDI_TERM	ENET_MDI2	37
1144		ENET_MDI_TERM	ENET_MDI3	37
ENET_MDI0	ENET_100D	ENET_MDI	ENET_MDI_P<0>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<0>	37 39
ENET_MDI1	ENET_100D	ENET_MDI	ENET_MDI_P<1>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<1>	37 39
ENET_MDI2	ENET_100D	ENET_MDI	ENET_MDI_P<2>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<2>	37 39
ENET_MDI3	ENET_100D	ENET_MDI	ENET_MDI_P<3>	37 39
	ENET_100D	ENET_MDI	ENET_MDI_N<3>	37 39

SB Constraints (2 of 2)

SYNC_MASTER=(MASTER) SYNC_DATE=(10/02/2006)

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Clock Signal Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
CLK_FSB_100D	*	100_OHM_DIFF
CLK_PCIE_100D	*	100_OHM_DIFF
CLK_MED_55S	*	55_OHM_SE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	*	*	CLK_SPACING_0.6MM
CLK_PCIE	*	*	CLK_SPACING_0.5MM
CLK_MED	*	*	CLK_SPACING_0.5MM

SOURCE: Santa Rosa Platform DG, Rev 1.0 (#21112), Sections 14.1 - 14.6

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_P	29 30
CK505_CPU	CLK_FSB_100D	CLK_FSB	CK505_CPU0_N	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_P	29 30
CK505_NB	CLK_FSB_100D	CLK_FSB	CK505_CPU1_N	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_P	29 30
CK505_ITP	CLK_FSB_100D	CLK_FSB	CK505_CPU2_ITP_SRC10_N	29 30
CK505_PCIF0	CLK_MED_55S	CLK_MED	CK505_PCIF0_CLK_ITPEN	29 30
CK505_PCIF1	CLK_MED_55S	CLK_MED	CK505_PCIF1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI1_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI2_CLK	29 30
CK505_PCI3	CLK_MED_55S	CLK_MED	CK505_PCI3_CLK	29 30
	CLK_MED_55S	CLK_MED	CK505_PCI4_CLK	29 30
CK505_PCI5	CLK_MED_55S	CLK_MED	CK505_PCI5_CLK_FCTSEL	29 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_48M_FSA	29 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_REF0_FSC	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_DOT96_27M_N	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_LVDS_N	29 30
CK505_SRC1	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC1_N	29 30
CK505_SRC2	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC2_N	29 30
CK505_SRC3	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC3_N	29 30
CK505_SRC4	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC4_N	29 30
CK505_SRC5	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC5_N	29 30
CK505_SRC6	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC6_N	29 30
CK505_SRC7	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC7_N	29 30
CK505_SRC8	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_P	29 30
	CLK_PCIE_100D	CLK_PCIE	CK505_SRC8_N	29 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_P	7 10 30
(CK505_CPU)	CLK_FSB_100D	CLK_FSB	FSB_CLK_CPU_N	7 10 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_P	7 14 30
(CK505_NB)	CLK_FSB_100D	CLK_FSB	FSB_CLK_NB_N	7 14 30
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_P	13 30 100
(CK505_ITP)	CLK_FSB_100D	CLK_FSB	XDP_CLK_N	13 30 100
(CK505_PCIF0)	CLK_MED_55S	CLK_MED	PCI_CLK33M_LPCPLUS	7 30 51
(CK505_PCIF1)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SB	7 24 30
(CK505_PCI2)	CLK_MED_55S	CLK_MED	PCI_CLK33M_TPM	
(CK505_PCI3)	CLK_MED_55S	CLK_MED	PCI_CLK33M_SMC	7 30 49
			CK505 PCI4 is project-specific	
			CK505 PCI5 is project-specific	
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	SB_CLK48M_USBCTLR	7 25 30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	SB_CLK14P3M_TIMER	7 25 30
(CPU_BSEL0)	CLK_MED_55S	CLK_MED	CK505_FSA	30
(CPU_BSEL2)	CLK_MED_55S	CLK_MED	CK505_FSC	30
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_P	30 85
(CK505_SRC1)	CLK_PCIE_100D	CLK_PCIE	GPU_CLK100M_PCIE_N	30 85
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_P	7 24 30
(CK505_SRC2)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_DMI_N	7 24 30
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_P	7 30 40
(CK505_SRC3)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_FW_N	7 30 40
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_P	7 23 30
(CK505_SRC4)	CLK_PCIE_100D	CLK_PCIE	SB_CLK100M_SATA_N	7 23 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_P	7 16 30
(CK505_SRC5)	CLK_PCIE_100D	CLK_PCIE	NB_CLK100M_PCIE_N	7 16 30
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_P	30 34
(CK505_SRC6)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_MINI_N	30 34
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_P	7 30 37
(CK505_SRC8)	CLK_PCIE_100D	CLK_PCIE	PCIE_CLK100M_ENET_N	7 30 37

Clock Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

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FireWire Interface Constraints

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
FW_110D	*	110_OHM_DIFF
FW_110D	BGA_P1MM	110_OHM_DIFF_ESCAPE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FW_TP	*	*	SPACING_0.3MM

FireWire Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
FW_0_TPA	FW_110D	FW_TP	FW_PORT0_TPA_P	43
	FW_110D	FW_TP	FW_PORT0_TPA_N	43
FW_0_TPB	FW_110D	FW_TP	FW_PORT0_TPB_P	43
	FW_110D	FW_TP	FW_PORT0_TPB_N	43
FW_1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_N	43
FW_1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_N	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPA_FL_N	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_P	43
	FW_110D	FW_TP	FW_PORT1_TPB_FL_N	43

Port 2 Not Used

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
SMBUS_SMC_A_S3_SCL	SMB_5SS	SMB	SMBUS_SMC_A_S3_SCL	
SMBUS_SMC_A_S3_SDA	SMB_5SS	SMB	SMBUS_SMC_A_S3_SDA	
SMBUS_SMC_B_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_B_S0_SCL	52
SMBUS_SMC_B_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_B_S0_SDA	52
SMBUS_SMC_0_S0_SCL	SMB_5SS	SMB	SMBUS_SMC_0_S0_SCL	52
SMBUS_SMC_0_S0_SDA	SMB_5SS	SMB	SMBUS_SMC_0_S0_SDA	52
SMBUS_SMC_BSA_SCL	SMB_5SS	SMB	SMBUS_SMC_BSA_SCL	52
SMBUS_SMC_BSA_SDA	SMB_5SS	SMB	SMBUS_SMC_BSA_SDA	52
SMBUS_SMC_MGMT_SCL	SMB_5SS	SMB	SMBUS_SMC_MGMT_SCL	52
SMBUS_SMC_MGMT_SDA	SMB_5SS	SMB	SMBUS_SMC_MGMT_SDA	52

FireWire & SMC Constraints

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	900
PWR	*	=STANDARD	900

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM
MEM_CLK	PWR	*	PWR_P2MM
MEM_CMD	PWR	*	PWR_P2MM
MEM_CTRL	PWR	*	PWR_P2MM
MEM_DATA	PWR	*	PWR_P2MM
MEM_DQS	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLINK_VREF	GND	*	GND_P2MM
CLK_MED	GND	*	GND_P2MM
CLK_PCIE	GND	*	GND_P2MM
DMI	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	PWR	*	PWR_P2MM
DMI	PWR	*	PWR_P2MM
SATA	PWR	*	PWR_P2MM
USB	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_FSB	GND	*	GND_P2MM
CPU_COMP	GND	*	GND_P2MM
CPU_GTLREF	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM
FSB_DSTB	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM
ENET_MDI	PWR	*	PWR_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_MED	PWR	*	GND_P2MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
THERM_DIFF	*	1:1_DIFFPAIR

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
THERMAL	*	*	SPACING_0.4MM
SWITCHNODE	*	*	SWITCHNODE
THERMAL	PWR	*	PWR_P2MM
THERMAL	GND	*	GND_P2MM
SMS	*	*	SPACING_0.3MM

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
TMDS_DATA	TMDS_100D	TMDS	TMDS_DATA_P<3..0>	85 94
	TMDS_100D	TMDS	TMDS_DATA_N<3..0>	85 94
TMDS_CLK	TMDS_100D	TMDS	TMDS_CLK_P	85 94
	TMDS_100D	TMDS	TMDS_CLK_N	85 94
	TMDS_100D	TMDS	TMDS_CONN_DP<3..0>	94
	TMDS_100D	TMDS	TMDS_CONN_DN<3..0>	94
	TMDS_100D	TMDS	TMDS_CONN_CLKP	94
	TMDS_100D	TMDS	TMDS_CONN_CLKN	94
(USB_EXTA)	USB_90D	USB	USB_PORT0_P	46
(USB_EXTA)	USB_90D	USB	USB_PORT0_N	46
(USB_EXTB)	USB_90D	USB	USB_PORT1_P	46
(USB_EXTB)	USB_90D	USB	USB_PORT1_N	46
(USB_EXTC)	USB_90D	USB	USB_PORT2_P	46
(USB_EXTC)	USB_90D	USB	USB_PORT2_N	46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_P	46
(USB_EXTD)	USB_90D	USB	USB_C_MUXED_N	46
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_P	47
(USB_CAMERA)	USB_90D	USB	USB_CAMERA_L_N	47
(USB_IR)	USB_90D	USB	USB_IR_L_P	47
(USB_IR)	USB_90D	USB	USB_IR_L_N	47
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_P	85 90
LVDS_A_CLK	LVDS_100D	LVDS	LVDS_L_CLK_N	85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_P<3..0>	85 90
LVDS_A_DATA	LVDS_100D	LVDS	LVDS_L_DATA_N<3..0>	85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_P	85 90
LVDS_B_CLK	LVDS_100D	LVDS	LVDS_U_CLK_N	85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_P<3..0>	85 90
LVDS_B_DATA	LVDS_100D	LVDS	LVDS_U_DATA_N<3..0>	85 90
	PCIE_100D	PCIE	PCIE_FW_R2D_N	7 40
	PCIE_100D	PCIE	PCIE_FW_R2D_P	7 40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_N	40
	PCIE_100D	PCIE	PCIE_FW_D2R_C_P	40
	PCIE_100D	PCIE	PCIE_ENET_R2D_P	7 37
	PCIE_100D	PCIE	PCIE_ENET_R2D_N	7 37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_100D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_100D	PCIE	PCIE_MINI_R2D_N	34
	PCIE_100D	PCIE	PCIE_MINI_R2D_P	34
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<0>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<0>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<1>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<1>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<2>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<2>	39
ENET_MDI_T	ENET_100D	ENET_MDI	ENET_MDI_T_P<3>	39
	ENET_100D	ENET_MDI	ENET_MDI_T_N<3>	39
	ENET_100D	ENET_MDI	ENET_MDI_R_P<0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<0>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<1>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<1>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<2>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<2>	
	ENET_100D	ENET_MDI	ENET_MDI_R_P<3>	
	ENET_100D	ENET_MDI	ENET_MDI_R_N<3>	
	CRT_50S	CRT	GPU_TV_COMP	85 91
	CRT_50S	CRT	GPU_TV_C	85 91
	CRT_50S	CRT	GPU_TV_Y	85 91
CRT_RED	CRT_50S	CRT	GPU_RED	85 91
CRT_GREEN	CRT_50S	CRT	GPU_GRN	85 91
CRT_BLUE	CRT_50S	CRT	GPU_BLU	85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_H2SYNC	85 91
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_V2SYNC	85 91
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_HSYNC	91 94
CRT_SYNC	CRT_55S	CRT_SYNC	VGA_VSYNC	91 94
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_HSYNC	
(CRT_SYNC)	CRT_55S	CRT_SYNC	GPU_BUF_VSYNC	
	CRT_50S	CRT	VIDEO_MUX_RED	91
	CRT_50S	CRT	VIDEO_MUX_GRN	91
	CRT_50S	CRT	VIDEO_MUX_BLU	91
	CRT_55S	CRT	VGA_RED	91 94
	CRT_55S	CRT	VGA_GRN	91 94
	CRT_55S	CRT	VGA_BLU	91 94
THERM_DIFF	THERM_DIFF	THERMAL	HDD_THRMD_P	55
	THERM_DIFF	THERMAL	HDD_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	ODD_THRMD_P	55
	THERM_DIFF	THERMAL	ODD_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_THERMD_P	10 55
	THERM_DIFF	THERMAL	CPU_THERMD_N	10 55
THERM_DIFF	THERM_DIFF	THERMAL	GPU_HSK_THRMD_P	55
	THERM_DIFF	THERMAL	GPU_HSK_THRMD_N	55
THERM_DIFF	THERM_DIFF	THERMAL	CPU_HSK_THRMD_P	55
	THERM_DIFF	THERMAL	CPU_HSK_THRMD_N	55

M72/M78 SPECIFIC NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		SWITCHNODE	IMVP6_PHASE1	71
		SWITCHNODE	IMVP6_PHASE2	71
		SWITCHNODE	IMVP6_PHASE3	72
		SWITCHNODE	1V05REG_SWITCHNODE	73
		SWITCHNODE	1V5REG_SWITCHNODE	73
		SWITCHNODE	MCH_CORES0_SWITCHNODE	74
		SWITCHNODE	1V25REG_SWITCHNODE	74
		SWITCHNODE	1V8S3_PHASE	75
		SWITCHNODE	5VS5_SW	76
		SWITCHNODE	3V3S3_SW	76
		SWITCHNODE	P3V3S5_SW	77
		SWITCHNODE	P2V5S0_SW	
		SMS	SMS_X_AXIS	49 50
		SMS	SMS_Y_AXIS	49 50
		SMS	SMS_Z_AXIS	49 50

M72/M78 SPECIFIC CONSTRAINTS

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

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M72/M78 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,BOTTOM	NO_TYPE,BGA_P1MM	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	4 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	12.7 MM	=DEFAULT	=DEFAULT
DEFAULT	TOP,BOTTOM	Y	=55_OHM_SE	0.100 MM	3 MM	0 MM	0 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.125 MM	0.125 MM			
55_OHM_SE	*	Y	0.100 MM	0.100 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.225 MM	0.225 MM			
40_OHM_SE	*	Y	0.185 MM	0.185 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
45_OHM_SE	*	Y	0.150 MM	0.150 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.340 MM	0.340 MM			
27P4_OHM_SE	*	Y	0.265 MM	0.265 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
70_OHM_DIFF	ISL3,ISL6	Y	0.180 MM	0.180 MM		0.120 MM	0.120 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.215 MM	0.215 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL6	Y	0.120 MM	0.120 MM		0.130 MM	0.130 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL6	Y	0.125 MM	0.125 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.145 MM	0.145 MM		0.175 MM	0.175 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL6	Y	0.095 MM	0.095 MM		0.205 MM	0.205 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.280 MM	0.280 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF_ESCAPE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF_ESCAPE	TOP,BOTTOM	Y	0.105 MM	0.100 MM		0.250 MM	0.250 MM
110_OHM_DIFF_ESCAPE	ISL3,ISL6	Y	0.085 MM	0.085 MM		0.330 MM	0.330 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.15 MM	0.15 MM			
50_OHM_SE	*	Y	0.120 MM	0.120 MM	=STANDARD	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?
BGA_P3MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA_P1MM	BGA_P1MM
MEM_CLK	*	BGA_P1MM	BGA_P2MM
CLK_FSB	*	BGA_P1MM	BGA_P2MM
CLK_PCIE	*	BGA_P1MM	BGA_P2MM
CLK_MED	*	BGA_P1MM	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA_P1MM	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPACING_0.15MM	*	0.15 MM	?
SPACING_0.18MM	*	0.18 MM	?
SPACING_0.2MM	*	0.2 MM	?
SPACING_0.25MM	*	0.25 MM	?
SPACING_0.3MM	*	0.3 MM	?
SPACING_0.4MM	*	0.4 MM	?
SPACING_0.5MM	*	0.5 MM	?
SPACING_0.6MM	*	0.6 MM	?
SWITCHNODE	*	0.6 MM	1000
SWITCHNODE	TOP,BOTTOM	0.2 MM	1000

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SPACING_0.5MM	*	0.5 MM	?
CLK_SPACING_0.6MM	*	0.6 MM	?
CLK_SPACING_0.5MM	TOP,BOTTOM	0.2 MM	?
CLK_SPACING_0.6MM	TOP,BOTTOM	0.2 MM	?

M72/M78 RULE DEFINITIONS

SYNC_MASTER=T9_MLB SYNC_DATE=09/27/2006

APPLE INC.

SIZE	DRAWING NUMBER	REV.
D	051-7388	A

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Title: Basenet Report
Design: k2
Date: Jan 8 14:39:56 2008

Base nets and synonyms for k2_lib.K2(@k2_lib.k2(sch_1))

Base Signal	Synonyms	Location([Zone][dir])
0V9S0_COMP_REF	0V9S0_COMP_REF - @k2_lib.K2	70C6
1V05REG_BOOT	1V05REG_BOOT - @k2_lib.K2	73C4
1V05REG_BOOT_R	1V05REG_BOOT_R - @k2_lib.K2	73C3
1V05REG_ISEN	1V05REG_ISEN - @k2_lib.K2	73C4
1V05REG_LGATE	1V05REG_LGATE - @k2_lib.K2	73C3
1V05REG_OCSET	1V05REG_OCSET - @k2_lib.K2	73B4
1V05REG_SNUBBER_R	1V05REG_SNUBBER_R - @k2_lib.K2	73C2
1V05REG_SOFT	1V05REG_SOFT - @k2_lib.K2	73C4
1V05REG_SWITCHNODE	1V05REG_SWITCHNODE - @k2_lib.K2	73B3 108D1
1V05REG_UGATE	1V05REG_UGATE - @k2_lib.K2	73C4
1V05REG_VSEN	1V05REG_VSEN - @k2_lib.K2	73B3
1V05S0_EN	1V05S0_EN - @k2_lib.K2	73B4
1V05S0_RUNSS	1V05S0_RUNSS - @k2_lib.K2	70C5 73C3 74C3
1V05S0_RUNSS_BUF	1V05S0_RUNSS_BUF - @k2_lib.K2	70C6
1V5REG_BOOT	1V5REG_BOOT - @k2_lib.K2	73C5
1V5REG_BOOT_R	1V5REG_BOOT_R - @k2_lib.K2	73C6
1V5REG_ISEN	1V5REG_ISEN - @k2_lib.K2	73C5
1V5REG_LGATE	1V5REG_LGATE - @k2_lib.K2	73C5
1V5REG_OCSET	1V5REG_OCSET - @k2_lib.K2	73B5
1V5REG_SNUBBER_R	1V5REG_SNUBBER_R - @k2_lib.K2	73B7
1V5REG_SOFT	1V5REG_SOFT - @k2_lib.K2	73C5
1V5REG_SWITCHNODE	1V5REG_SWITCHNODE - @k2_lib.K2	73C6 108D1
1V5REG_UGATE	1V5REG_UGATE - @k2_lib.K2	73C5
1V5REG_VSEN	1V5REG_VSEN - @k2_lib.K2	73B7
1V5S0_RUNSS	1V5S0_RUNSS - @k2_lib.K2	70A5 73C5
1V5S0_RUNSS_BUF	1V5S0_RUNSS_BUF - @k2_lib.K2	70A6
1V8S0_COMP_REF	1V8S0_COMP_REF - @k2_lib.K2	70D6
1V8S3_BOOT	1V8S3_BOOT - @k2_lib.K2	75C5
1V8S3_BOOT_RC	1V8S3_BOOT_RC - @k2_lib.K2	75D5
1V8S3_COMP	1V8S3_COMP - @k2_lib.K2	75C6
1V8S3_COMP_R	1V8S3_COMP_R - @k2_lib.K2	75C6
1V8S3_EN	1V8S3_EN - @k2_lib.K2	75C6
1V8S3_FB	1V8S3_FB - @k2_lib.K2	75C6
1V8S3_FCCM	1V8S3_FCCM - @k2_lib.K2	75C6
1V8S3_FSET	1V8S3_FSET - @k2_lib.K2	75C6
1V8S3_ISEN	1V8S3_ISEN - @k2_lib.K2	75C5
1V8S3_LG	1V8S3_LG - @k2_lib.K2	75C5
1V8S3_PHASE	1V8S3_PHASE - @k2_lib.K2	75C5 108D1
1V8S3_SNUBBER_R	1V8S3_SNUBBER_R - @k2_lib.K2	75C3
1V8S3_UG	1V8S3_UG - @k2_lib.K2	75C5
1V8S3_VCC	1V8S3_VCC - @k2_lib.K2	75D6
1V25REG_BOOT	1V25REG_BOOT - @k2_lib.K2	74C5
1V25REG_BOOT_R	1V25REG_BOOT_R - @k2_lib.K2	74C6
1V25REG_ISEN	1V25REG_ISEN - @k2_lib.K2	74C5
1V25REG_LGATE	1V25REG_LGATE - @k2_lib.K2	74C5
1V25REG_OCSET	1V25REG_OCSET - @k2_lib.K2	74B5
1V25REG_SNUBBER_R	1V25REG_SNUBBER_R - @k2_lib.K2	74B7
1V25REG_SOFT	1V25REG_SOFT - @k2_lib.K2	74C5
1V25REG_SWITCHNODE	1V25REG_SWITCHNODE - @k2_lib.K2	74C6 108D1
1V25REG_UGATE	1V25REG_UGATE - @k2_lib.K2	74C5
1V25REG_VSEN	1V25REG_VSEN - @k2_lib.K2	74B7
1V25S0_RUNSS	1V25S0_RUNSS - @k2_lib.K2	70B5 74C5
1V25S0_RUNSS_BUF	1V25S0_RUNSS_BUF - @k2_lib.K2	70B6
3V3S0_COMP_REF	3V3S0_COMP_REF - @k2_lib.K2	70D6
3V3S3_BG	3V3S3_BG - @k2_lib.K2	76B5
3V3S3_BOOST	3V3S3_BOOST - @k2_lib.K2	76B5
3V3S3_BOOST_R	3V3S3_BOOST_R - @k2_lib.K2	76C6
3V3S3_ITH	3V3S3_ITH - @k2_lib.K2	76B5
3V3S3_ITH_R	3V3S3_ITH_R - @k2_lib.K2	76B6
3V3S3_RUNSS	3V3S3_RUNSS - @k2_lib.K2	76B5
3V3S3_SNS_N	3V3S3_SNS_N - @k2_lib.K2	76C6
3V3S3_SNS_P	3V3S3_SNS_P - @k2_lib.K2	76C6
3V3S3_SW	3V3S3_SW - @k2_lib.K2	76B5 108D1
3V3S3_TG	3V3S3_TG - @k2_lib.K2	76C5
3V3S3_VOSNS	3V3S3_VOSNS - @k2_lib.K2	76B5
5VS0_COMP_REF	5VS0_COMP_REF - @k2_lib.K2	70C6
5VS3_COMP_REF	5VS3_COMP_REF - @k2_lib.K2	76A7
5VS5_0V76_REF	5VS5_0V76_REF - @k2_lib.K2	70C6
5VS5_1V53_REF	5VS5_1V53_REF - @k2_lib.K2	70D6
5VS5_2V80_REF	5VS5_2V80_REF - @k2_lib.K2	70D6
5VS5_4V24_REF1	5VS5_4V24_REF1 - @k2_lib.K2	70D6
5VS5_4V24_REF2	5VS5_4V24_REF2 - @k2_lib.K2	76A7
5VS5_4V29_REF	5VS5_4V29_REF - @k2_lib.K2	76D7
5VS5_BG	5VS5_BG - @k2_lib.K2	76B4
5VS5_BOOST	5VS5_BOOST - @k2_lib.K2	76B4
5VS5_BOOST_R	5VS5_BOOST_R - @k2_lib.K2	76C3
5VS5_ITH	5VS5_ITH - @k2_lib.K2	76B4
5VS5_ITH_R	5VS5_ITH_R - @k2_lib.K2	76B3
5VS5_RUNSS	5VS5_RUNSS - @k2_lib.K2	76B4
5VS5_SNS_N	5VS5_SNS_N - @k2_lib.K2	76C3
5VS5_SNS_P	5VS5_SNS_P - @k2_lib.K2	76C3
5VS5_SW	5VS5_SW - @k2_lib.K2	76B4 108D1
5VS5_TG	5VS5_TG - @k2_lib.K2	76C4
5VS5_VOSNS	5VS5_VOSNS - @k2_lib.K2	76B4
12VS0_6V0_REF	12VS0_6V0_REF - @k2_lib.K2	76D7
12VS0_COMP_REF	12VS0_COMP_REF - @k2_lib.K2	76D7
=ENET_VMAIN_AVLBL	=ENET_VMAIN_AVLBL - @k2_lib.K2	37C2 38B3
	PP3V3_S0 - @k2_lib.K2	6B8 6C6 6D7 7D3 13D6 53C3 70C3 70D3 70D8 77B6 78C1
	=PP3V3_DDC_LCD - @k2_lib.K2	90A8 90D5
	=PP3V3_S0_VIDEO - @k2_lib.K2	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_NB_VCCA_PEG_BG - @k2_lib.K2	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @k2_lib.K2	6A4 21C2
	=PP3V3_S0_TSENS - @k2_lib.K2	6A4 55B5 55D5 55D5 55D6 55D8
	=PP3V3_S0_SMC - @k2_lib.K2	6A4 53D5
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @k2_lib.K2	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @k2_lib.K2	6A4 26A3 27D4
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @k2_lib.K2	6B4 26C3
	=PP3V3R1V5_S0_SB_VCCHDA - @k2_lib.K2	6B4 26B3 27B4
	=PP3V3_S0_SB_VCC3_3_DMI - @k2_lib.K2	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_SATA - @k2_lib.K2	6B4 26C3 27C4
	=PP3V3_S0MWOL_SB_CLINK0 - @k2_lib.K2	6B4 25C1
	=PP3V3_S0M_CK505 - @k2_lib.K2	6B4 29D2 29D8 30D1
	=PP3V3_S0_SATALED - @k2_lib.K2	6B4 45C3
	=PP3V3_S0_MXM - @k2_lib.K2	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_CK505 - @k2_lib.K2	6B4 29C7 30D7
	=PP3V3_S0_SMBUS_SMC_B_S0 - @k2_lib.K2	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_MGMT - @k2_lib.K2	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_0_S0 - @k2_lib.K2	6B4 52D5
	=PP3V3_S0_SMC_LS - @k2_lib.K2	6B4 50D2
	=PP3V3_S0_LPCPLUS - @k2_lib.K2	6B4 51C4
	=PP3V3_S0_SMBUS_SB - @k2_lib.K2	6B4 52D8
	=PP3V3_S0_IMVP - @k2_lib.K2	6B4 71D8
	=PP3V3_S0_AUDIO - @k2_lib.K2	6B4 98C4 98C6
	=PPSPD_S0_MEM - @k2_lib.K2	6B4 31A7 32A3 32A7
	=PP3V3_S0_FAN - @k2_lib.K2	6B4 56B7 56C7 57C7
	=PP3V3_S0_SB_PM - @k2_lib.K2	6B4 28A7
	=PP3V3_S0_PATA - @k2_lib.K2	6B4 44C6
	=PP3V3_S0_SB_PCI - @k2_lib.K2	6B4 24A3
	=PP3V3_S0_SB_VCC3_3_IDE - @k2_lib.K2	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_PCI - @k2_lib.K2	6B4 26B3 27C4
	=PP3V3_S0_SB_GPIO - @k2_lib.K2	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @k2_lib.K2	6B4 26A6
	=PP3V3_S0_SB - @k2_lib.K2	6C4 27D8
	=PP3V3_S0_NB_VCCHV - @k2_lib.K2	6C4 16B7 16C7 16C7 19B3 21A8
	PP3V3_S0 - @k2_lib.K2	6B8 6C6 6D7 7D3 13D6 53C3 70C3 70D3 70D8 77B6 78C1
	=PPSPD_S0_MEM - @k2_lib.K2	6B4 31A7 32A3 32A7
	=PP3V3_S0_VIDEO - @k2_lib.K2	6A4 90D7 91B4 91B4 91B7 94D2
	=PP3V3_S0_TSENS - @k2_lib.K2	6A4 55B5 55D5 55D5 55D6 55D8
	=PP3V3_S0_SMC_LS - @k2_lib.K2	6B4 50D2
	=PP3V3_S0_SMC - @k2_lib.K2	6A4 53D5
	=PP3V3_S0_SMBUS_SMC_MGMT - @k2_lib.K2	6B4 52B3
	=PP3V3_S0_SMBUS_SMC_B_S0 - @k2_lib.K2	6B4 52C5
	=PP3V3_S0_SMBUS_SMC_0_S0 - @k2_lib.K2	6B4 52D5
	=PP3V3_S0_SMBUS_SB - @k2_lib.K2	6B4 52D8
	=PP3V3_S0_SB_VCCGLAN3_3 - @k2_lib.K2	6B4 26A6
	=PP3V3_S0_SB_VCC3_3_VCCPCORE - @k2_lib.K2	6B4 26C3
	=PP3V3_S0_SB_VCC3_3_SATA - @k2_lib.K2	6B4 26C3 27C4
	=PP3V3_S0_SB_VCC3_3_PCI - @k2_lib.K2	6B4 26B3 27C4
	=PP3V3_S0_SB_VCC3_3_IDE - @k2_lib.K2	6B4 26C3 27D4
	=PP3V3_S0_SB_VCC3_3_DMI - @k2_lib.K2	6B4 26C3 27C4
	=PP3V3_S0_SB_PM - @k2_lib.K2	6B4 28A7
	=PP3V3_S0_SB_PCI - @k2_lib.K2	6B4 24A3
	=PP3V3_S0_SB_GPIO - @k2_lib.K2	6B4 23D2 23D7 25B3 25D8
	=PP3V3_S0_SB - @k2_lib.K2	6C4 27D8
	=PP3V3_S0_SATALED - @k2_lib.K2	6B4 45C3
	=PP3V3_S0_PATA - @k2_lib.K2	6B4 44C6
	=PP3V3_S0_NB_VCCHV - @k2_lib.K2	6C4 16B7 16C7 16C7 19B3 21A8
	=PP3V3_S0_NB_VCCA_PEG_BG - @k2_lib.K2	6A4 19C6 21A6
	=PP3V3_S0_NB_FOLLOW - @k2_lib.K2	6A4 21C2
	=PP3V3_S0_MXM - @k2_lib.K2	6B4 85A3 85C4 85C8 85C8 85D2
	=PP3V3_S0_LPCPLUS - @k2_lib.K2	6B4 51C4
	=PP3V3_S0_IMVP - @k2_lib.K2	6B4 71D8
	=PP3V3_S0_FAN - @k2_lib.K2	6B4 56B7 56C7 57C7
	=PP3V3_S0_ENET - @k2_lib.K2	6A4 38B1
	=PP3V3_S0_CK505 - @k2_lib.K2	6B4 29C7 30D7
	=PP3V3_S0_AUDIO - @k2_lib.K2	6B4 98C4 98C6
	=PP3V3_S0M_CK505 - @k2_lib.K2	6B4 29D2 29D8 30D1
	=PP3V3_S0MWOL_SB_VCCLAN3_3 - @k2_lib.K2	6A4 26A3 27D4
	=PP3V3_S0MWOL_SB_VCCCL3_3 - @k2_lib.K2	6A4 26A6 27D4
	=PP3V3_S0MWOL_SB_CLINK0 - @k2_lib.K2	6B4 25C1
	=PP3V3R1V5_S0_SB_VCCHDA - @k2_lib.K2	6B4 26B3 27B4
=GFX_VR_EN	=GFX_VR_EN - @k2_lib.K2	16B3 22A8
	TP_GFX_VR_EN - @k2_lib.K2	22A7
=GND_NB_VSSA_LVDS	=GND_NB_VSSA_LVDS - @k2_lib.K2	19C6 22C1
	TP_NB_VSSA_LVDS - @k2_lib.K2	22C2
=NB_CLINK_MPWROK	=NB_CLINK_MPWROK - @k2_lib.K2	16A3 22C2
	VR_PWRGOOD_DELAY - @k2_lib.K2	7C4 7C7 16B6 22C1 70C2 71C7
=PP0V9_S0M_MEM_TERM	=PP0V9_S0M_MEM_TERM - @k2_lib.K2	6D4 33D5
	PP0V9_S0 - @k2_lib.K2	6D6 7D3 70C8 75A3
=PP0V9_S3M_MEM_NBVREFA	=PP0V9_S3M_MEM_NBVREFA - @k2_lib.K2	7C7 16C2 22B1
	PP0V9_S3M_MEM_NBVREFA - @k2_lib.K2	22B2
=PP0V9_S3M_MEM_NBVREFB	=PP0V9_S3M_MEM_NBVREFB - @k2_lib.K2	7C7 16C2 22A1
	PP0V9_S3M_MEM_NBVREFB - @k2_lib.K2	22A2
=PP0V9_S3_MEM_A_VREF	=PP0V9_S3_MEM_A_VREF - @k2_lib.K2	31C1 31D6
	PP0V9_S3_MEM_A_VREF - @k2_lib.K2	31C2
=PP0V9_S3_MEM_B_VREF	=PP0V9_S3_MEM_B_VREF - @k2_lib.K2	32C1 32D7
	PP0V9_S3_MEM_B_VREF - @k2_lib.K2	32C2
=PP1V2_ENET_PHY	=PP1V2_ENET_PHY - @k2_lib.K2	37D6 38A3
	PP1V2_S3_ENET - @k2_lib.K2	38A3
=PP1V05_S0M_NB_VCCAXM	=PP1V05_S0M_NB_VCCAXM - @k2_lib.K2	6C4 18B3 18C1 21D8
	=PP1V05_S0_NB_FOLLOW - @k2_lib.K2	6C4 21C4
	=PPVCORE_S0_SB - @k2_lib.K2	6C4 26D3 27B1
	PP1V05_S0 - @k2_lib.K2	6C6 7D3 34C3 73A4 73C1
	=PP1V05_S0_NB_PCIE - @k2_lib.K2	6C4 21D5
	PP1V05_S0 - @k2_lib.K2	6C6 7D3 34C3 73A4 73C1
	=PPVCORE_S0_SB - @k2_lib.K2	6C4 26D3 27B1
	=PP1V05_S0_NB_PCIE - @k2_lib.K2	6C4 21D5
	=PP1V05_S0_NB_FOLLOW - @k2_lib.K2	6C4 21C4
=PP1V05_S0_CPU	=PP1V05_S0_CPU - @k2_lib.K2	6D4 10B5 10B6 10C5 10D5 11C6 12A3 13D6 50D2
	=PP1V05_S0_SB_CPU_IO - @k2_lib.K2	6C4 23D2 26C3 27B2
	=PPVCORE_S0_NB_FOLLOW - @k2_lib.K2	6D4 21B4
	PPMCH_CORE_S0 - @k2_lib.K2	6D6 7D3 55A6 73A2 74C1
	=PP1V25R1V05_S0_NB_VTT - @k2_lib.K2	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @k2_lib.K2	6D4 14B7 30B8 30C8 30C8
	=PPVCORE_S0_NB - @k2_lib.K2	6D4 18D3 18D7 21D8
	PPMCH_CORE_S0 - @k2_lib.K2	6D6 7D3 55A6 73A2 74C1
	=PPVCORE_S0_NB_FOLLOW - @k2_lib.K2	6D4 21B4
	=PPVCORE_S0_NB - @k2_lib.K2	6D4 18D3 18D7 21D8
	=PP1V25R1V05_S0_NB_VTT - @k2_lib.K2	6D4 19D3 21C8
	=PP1V25R1V05_S0_FSB_NB - @k2_lib.K2	6D4 14B7 30B8 30C8 30C8
	=PP1V05_S0_SB_CPU_IO - @k2_lib.K2	6C4 23D2 26C3 27B2
=PP1V5_S0_CPU	=PP1V5_S0_CPU - @k2_lib.K2	6C4 11B6 12B3
	=PP1V5_S0_MINI - @k2_lib.K2	6C4 34C2
	PP1V5_S0 - @k2_lib.K2	6C6 7D3 73C8
	=PP1V5_S0_SB - @k2_lib.K2	6C4 27C8
	PP1V5_S0_SB_VCCGLANPLL - @k2_lib.K2	26A6 27B6
	=PP1V5_S0_SB_VCC1_5_A - @k2_lib.K2	6C4 26B6
	=PP1V5_S0_SB_VCCUSBPLL - @k2_lib.K2	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @k2_lib.K2	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @k2_lib.K2	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @k2_lib.K2	6C4 26B6 27D2
	=PP1V5_S0_NB_TVDAC - @k2_lib.K2	6C4 22B3
	PP1V5_S0 - @k2_lib.K2	6C6 7D3 73C8
	=PP1V5_S0_SB_VCCUSBPLL - @k2_lib.K2	6C4 26A6 27C2
	=PP1V5_S0_SB_VCC1_5_A_USB_CORE - @k2_lib.K2	6C4 26B6 27C2
	=PP1V5_S0_SB_VCC1_5_A_ATX - @k2_lib.K2	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A_ARX - @k2_lib.K2	6C4 26B6 27D2
	=PP1V5_S0_SB_VCC1_5_A - @k2_lib.K2	6C4 26B6
	=PP1V5_S0_SB - @k2_lib.K2	6C4 27C8
	=PP1V5_S0_NB_TVDAC - @k2_lib.K2	6C4 22B3
	=PP1V5_S0_MINI - @k2_lib.K2	6C4 34C2
=PP1V5_S0_SB_VCCGLAN1_5	=PP1V5_S0_SB_VCCGLAN1_5 - @k2_lib.K2	26A6 27B6
	PP1V5_S0_SB_VCC1_5_B - @k2_lib.K2	23D7 24C2 26D6 27C6
=PP1V8_S0_MXM	=PP1V8_S0_MXM - @k2_lib.K2	6D4 84C8
	PP1V8_S0 - @k2_lib.K2	6D6 7D3 70D8 78B5
=PP1V8_S3M_MEM_NB	=PP1V8_S3M_MEM_NB - @k2_lib.K2	6D3 16D2 18D7 21C8 22B3
	=PP1V8_S3M_NB_VCC - @k2_lib.K2	6D3 21A4
	=PP1V8_S3_ENET - @k2_lib.K2	6D3 38B7
	PP1V8_S3 - @k2_lib.K2	6D4 7D3 75B3 75C1 78C6
	=PP1V8_S3_MEMVTT - @k2_lib.K2	6D3 75B6
	=PP1V8_S3_MEM - @k2_lib.K2	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	PP1V8_S3 - @k2_lib.K2	6D4 7D3 75B3 75C1 78C6
	=PP1V8_S3_MEMVTT - @k2_lib.K2	6D3 75B6
	=PP1V8_S3_MEM - @k2_lib.K2	6D3 31B2 31D2 31D3 31D6 32B2 32D2 32D3 32D6
	=PP1V8_S3_ENET - @k2_lib.K2	6D3 38B7
	=PP1V8_S3M_NB_VCC - @k2_lib.K2	6D3 21A4
=PP1V25_S0M_NB_PLL	=PP1V25_S0M_NB_PLL - @k2_lib.K2	6C4 21D3
	=PP1V25_S0M_NB_VCCD_HPLL - @k2_lib.K2	19A6 21D1
	=PP1V25_S0_SB_DMI - @k2_lib.K2	6C4 26C3 27C1
	PP1V25_S0 - @k2_lib.K2	6C6 7D3 74C8
	=PP1V25_S0_NB_VCC - @k2_lib.K2	6C4 21D5
	=PP1V25_S0_NB_PLL - @k2_lib.K2	6C4 21B4
	=PP1V25_S0M_NB_VCC - @k2_lib.K2	6C4 21A8
	=PP1V25_S0M_NB_VCCA - @k2_lib.K2	6C4 21B8
	=PP1V25_S0_NB_VCCDMI - @k2_lib.K2	6C4 19C3 21A8
	PP1V25_S0 - @k2_lib.K2	6C6 7D3 74C8
	=PP1V25_S0_SB_DMI - @k2_lib.K2	6C4 26C3 27C1
	=PP1V25_S0_NB_VCCDMI - @k2_lib.K2	6C4 19C3 21A8
	=PP1V25_S0_NB_VCC - @k2_lib.K2	6C4 21D5
	=PP1V25_S0_NB_PLL - @k2_lib.K2	6C4 21B4
	=PP1V25_S0M_NB_VCCA - @k2_lib.K2	6C4 21B8
	=PP1V25_S0M_NB_VCC - @k2_lib.K2	6C4 21A8
=PP2V5_S0_MXM	=PP2V5_S0_MXM - @k2_lib.K2	6D4 85A3
	PP2V5_S0 - @k2_lib.K2	6D6 7D3 77B4
=PP3V3_ENET_PHY	=PP3V3_ENET_PHY - @k2_lib.K2	37D6 38D6
	=PP3V3_S3_ENET - @k2_lib.K2	6D3 38C7 39A8
	=PP3V3_S3_BT - @k2_lib.K2	6D3 47D3
	=PP3V3_S3_MINI - @k2_lib.K2	6D3 34D2
	PP3V3_S3 - @k2_lib.K2	6A7 6D4 7D3 70D2 75D7 76B8 78C4
	=PP3V3_S3_MINI - @k2_lib.K2	6D3 34D2
	=PP3V3_S3_ENET - @k2_lib.K2	6D3 38C7 39A8
	=PP3V3_S3_BT - @k2_lib.K2	6D3 47D3
=PP3V3_S5_FAN	=PP3V3_S5_FAN - @k2_lib.K2	6D1 56B7 56D7 57D7
	=PP3V3_S5_SMBUS_SMC_A_S5 - @k2_lib.K2	6D1 52D3
	PP3V3_S5 - @k2_lib.K2	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @k2_lib.K2	6D1 46D5
	=PP3V3_S5_SMBUS_SMC_BSA - @k2_lib.K2	6D1 52C3
	=PP3V3_S5_LPCPLUS - @k2_lib.K2	6D1 7D4 51C6
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @k2_lib.K2	6D1 26B3 27B4
	=PP3V3_S5_SB_CLINK1 - @k2_lib.K2	6D1 25B1
	=PP3V3_S5_SB_GPIO - @k2_lib.K2	6D1 25D8
	=PP3V3_S5_ROM - @k2_lib.K2	6D1 61C6
	=PP3V3_S5_SMC - @k2_lib.K2	6D1 49D4 50B1 50D7
	=PP3V3_S5_FW - @k2_lib.K2	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
	=PP3V3_S5_SMBUS_SB_ME - @k2_lib.K2	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @k2_lib.K2	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @k2_lib.K2	6D1 26A3 27D5
	=PP3V3_S5_SB_PM - @k2_lib.K2	6D1 28A5
	=PP3V3_S5_SB_USB - @k2_lib.K2	6D1 24C8
	=PP3V3_S5_SB - @k2_lib.K2	6D1 25A3 25A8 27D8 28D7
	PP3V3_S5 - @k2_lib.K2	6A8 6D2 7C3 70B3 70C7 70D3 75D8 77D3
	=PP3V3_S5_SMCUSBMUX - @k2_lib.K2	6D1 46D5
	=PP3V3_S5_SMC - @k2_lib.K2	6D1 49D4 50B1 50D7
	=PP3V3_S5_SMBUS_SMC_BSA - @k2_lib.K2	6D1 52C3
	=PP3V3_S5_SMBUS_SMC_A_S5 - @k2_lib.K2	6D1 52D3
	=PP3V3_S5_SMBUS_SB_ME - @k2_lib.K2	6D1 52A8
	=PP3V3_S5_SB_VCCSUS3_3_USB - @k2_lib.K2	6D1 26A3 27C5
	=PP3V3_S5_SB_VCCSUS3_3 - @k2_lib.K2	6D1 26A3 27D5
	=PP3V3_S5_SB_USB - @k2_lib.K2	6D1 24C8
	=PP3V3_S5_SB_PM - @k2_lib.K2	6D1 28A5
	=PP3V3_S5_SB_GPIO - @k2_lib.K2	6D1 25D8
	=PP3V3_S5_SB_CLINK1 - @k2_lib.K2	6D1 25B1
	=PP3V3_S5_SB_3V3_VCCSUSHDA - @k2_lib.K2	6D1 26B3 27B4
	=PP3V3_S5_SB - @k2_lib.K2	6D1 25A3 25A8 27D8 28D7
	=PP3V3_S5_ROM - @k2_lib.K2	6D1 61C6
	=PP3V3_S5_LPCPLUS - @k2_lib.K2	6D1 7D4 51C6
	=PP3V3_S5_FW - @k2_lib.K2	6D1 40C2 40D3 40D4 42B3 42B6 42B8 42C8 42D3 43A8
=PP5V_S0_AUDIO	=PP5V_S0_AUDIO - @k2_lib.K2	6A4 98C4 98C6
	=PP5V_S0_MXM - @k2_lib.K2	6A4 84C8
	=PPV_S0_LCD_20INCH - @k2_lib.K2	6A4 90C8
	PP5V_S0 - @k2_lib.K2	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D1 94D6
	=PP5V_S0_SATA - @k2_lib.K2	6A4 6D6
	=PP5V_S0_LPCPLUS - @k2_lib.K2	6A4 7D4 51C6
	=PP5V_S0_PATA - @k2_lib.K2	6A4 44B6 44D6
	=PP5V_S0_SB - @k2_lib.K2	6A4 27D8
	PP5V_S0 - @k2_lib.K2	6A6 7D3 70C8 71D8 72D7 73C7 74C7 78D1 94D6
	=PPV_S0_LCD_20INCH - @k2_lib.K2	6A4 90C8
	=PP5V_S0_SB - @k2_lib.K2	6A4 27D8
	=PP5V_S0_PATA - @k2_lib.K2	6A4 44B6 44D6
	=PP5V_S0_MXM - @k2_lib.K2	6A4 84C8
	=PP5V_S0_LPCPLUS - @k2_lib.K2	6A4 7D4 51C6
=PP5V_S3_BNDI	=PP5V_S3_BNDI - @k2_lib.K2	6C3 47A3 47D7
	=PP5V_S3_MEMVTT - @k2_lib.K2	6C3 75B6
	PP5V_S3 - @k2_lib.K2	6C4 7D3 70D3 75D8 76A8 78D5
	=PP5V_S3_MEMVTT - @k2_lib.K2	6C3 75B6
=PP5V_S5_SB	=PP5V_S5_SB - @k2_lib.K2	6C1 27D8
	=PP5V_S5_USB - @k2_lib.K2	6C1 46C8 46D8
	PP5V_S5 - @k2_lib.K2	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78C7 78D4 78D7
	=PPVIN_S5_SMCVREF - @k2_lib.K2	6C1 50B8
	PP5V_S5 - @k2_lib.K2	6C2 7C3 70A7 70D8 76A8 76B1 76B5 76D8 77D6 78C7 78D4 78D7
	=PPVIN_S5_SMCVREF - @k2_lib.K2	6C1 50B8
	=PP5V_S5_USB - @k2_lib.K2	6C1 46C8 46D8
=PP12V_S0_AUDIO_SPKRAMP	=PP12V_S0_AUDIO_SPKRAMP - @k2_lib.K2	6A4 98C6
	=PP12V_S0_CPU - @k2_lib.K2	6A4 53B8 71D8 72D7
	=PPV_S0_LCD_24INCH - @k2_lib.K2	6A4 90C8
	=PPV_S0_MXM_PWRSRC - @k2_lib.K2	6A4 53D4
	PP12V_S0 - @k2_lib.K2	6A6 7D3 53B3 53B4 73D7 74D7 76D8
	=PP12V_S0_FAN - @k2_lib.K2	6A4 56B6 56D7 57D6
	PP12V_S0 - @k2_lib.K2	6A6 7D3 53B3 53B4 73D7 74D7 76D8
	=PPV_S0_MXM_PWRSRC - @k2_lib.K2	6A4 53D4
	=PPV_S0_LCD_24INCH - @k2_lib.K2	6A4 90C8
	=PP12V_S0_FAN - @k2_lib.K2	6A4 56B6 56D7 57D6
	=PP12V_S0_CPU - @k2_lib.K2	6A4 53B8 71D8 72D7
=PP12V_S5_FET	=PP12V_S5_FET - @k2_lib.K2	6C1
	PP12V_S5 - @k2_lib.K2	6C2 7C3 53B5 53C4 70D8 75D8 76A8 76D5 76D8
	=PP12V_S5_FW - @k2_lib.K2	6C1 43D8
	PP12V_S5 - @k2_lib.K2	6C2 7C3 53B5 53C4 70D8 75D8 76A8 76D5 76D8
	=PP12V_S5_FW - @k2_lib.K2	6C1 43D8
=PPVCORE_S0_CPU	=PPVCORE_S0_CPU - @k2_lib.K2	6D4 11B5 11D6 12D7 53B6 53D8
	PPVCORE_CPU - @k2_lib.K2	6D6 7D3 71D1 72C1
=SB_CLINK_MPWROK	=SB_CLINK_MPWROK - @k2_lib.K2	25C3 28B7
	PM_SB_PWROK - @k2_lib.K2	7C4 7C4 25C3 28B6 70C1
=SMC_SMS_INT	=SMC_SMS_INT - @k2_lib.K2	49B5 50B2
	SMC_SMS_INT - @k2_lib.K2	50B2
ACDC_TEMP	ACDC_TEMP - @k2_lib.K2	6D6 50C2
	SMC_ANALOG_ID - @k2_lib.K2	49A8 50C3
ALL_SYS_PWRGD	ALL_SYS_PWRGD - @k2_lib.K2	7C4 7C4 49D8 50C2 70C1 84C7
	PM_LAN_PWRGD - @k2_lib.K2	49C5 50C3
ALS_GAIN	ALS_GAIN - @k2_lib.K2	49A5 50D5
	NC_ALS_GAIN - @k2_lib.K2	50D3
ALS_LEFT	ALS_LEFT - @k2_lib.K2	49A8 50D5
	TP_ALS_LEFT - @k2_lib.K2	50D3
ALS_RIGHT	ALS_RIGHT - @k2_lib.K2	49A8 50D5
	TP_ALS_RIGHT - @k2_lib.K2	50D3
CK505_48M_FSA	CK505_48M_FSA - @k2_lib.K2	29A3 30C8 105D3
CK505_CLKREQ1_L	CK505_CLKREQ1_L - @k2_lib.K2	29B3 30D2 85C8
CK505_CLKREQ3_L	CK505_CLKREQ3_L - @k2_lib.K2	29B3 30D2 40C3
CK505_CLKREQ6_L	CK505_CLKREQ6_L - @k2_lib.K2	29B3 30C2
	MINI_CLKREQ_L - @k2_lib.K2	30C2 34C6
CK505_CLKREQ8_L	CK505_CLKREQ8_L - @k2_lib.K2	29A3 30C2
	ENET_CLKREQ_L - @k2_lib.K2	30C2 37B8
CK505_CPU0_N	CK505_CPU0_N - @k2_lib.K2	29C3 30D5 105D3
	FSB_CLK_CPU_N - @k2_lib.K2	7C8 10B6 30D3 105C3
CK505_CPU0_P	CK505_CPU0_P - @k2_lib.K2	29C3 30D5 105D3
	FSB_CLK_CPU_P - @k2_lib.K2	7C8 10B6 30D3 105C3
CK505_CPU1_N	CK505_CPU1_N - @k2_lib.K2	29C3 30D5 105D3
	FSB_CLK_NB_N - @k2_lib.K2	7C3 7C7 14B3 30D3 105C3
CK505_CPU1_P	CK505_CPU1_P - @k2_lib.K2	29C3 30D5 105D3
	FSB_CLK_NB_P - @k2_lib.K2	7C7 14B3 30D3 105C3
CK505_CPU2_ITP_SRC10_N	CK505_CPU2_ITP_SRC10_N - @k2_lib.K2	29C3 30D5 105D3
	XDP_CLK_N - @k2_lib.K2	13B3 30D3 100A3 105C3
CK505_CPU2_ITP_SRC10_P	CK505_CPU2_ITP_SRC10_P - @k2_lib.K2	29C3 30D5 105D3
	XDP_CLK_P - @k2_lib.K2	13C3 30D3 100A3 105C3
CK505_DOT96_27M_N	CK505_DOT96_27M_N - @k2_lib.K2	29A3 30A5 105D3
	TP_CK505_27M_N - @k2_lib.K2	30A3
CK505_DOT96_27M_P	CK505_DOT96_27M_P - @k2_lib.K2	29A3 30A5 105D3
	TP_CK505_27M_P - @k2_lib.K2	30A3
CK505_FSA	CK505_FSA - @k2_lib.K2	30C7 105B3
CK505_FSB_TEST_MODE	CK505_FSB_TEST_MODE - @k2_lib.K2	29C5 30B8
CK505_FSC	CK505_FSC - @k2_lib.K2	30B7 105B3
CK505_LVDS_N	CK505_LVDS_N - @k2_lib.K2	29C3 30C5 105C3
	TP_CK505_LVDS_N - @k2_lib.K2	30C3
CK505_LVDS_P	CK505_LVDS_P - @k2_lib.K2	29B3 30C5 105D3
	TP_CK505_LVDS_P - @k2_lib.K2	30C3
CK505_PCI1_CLK	CK505_PCI1_CLK - @k2_lib.K2	29C5 30A5 105D3
	TP_CK505_PCI1_CLK - @k2_lib.K2	7C3 30A3
CK505_PCI2_CLK	CK505_PCI2_CLK - @k2_lib.K2	29B5 30A5 105D3
	TP_PCI_CLK33M_TPM - @k2_lib.K2	30A3
CK505_PCI3_CLK	CK505_PCI3_CLK - @k2_lib.K2	29B5 30A5 105D3
CK505_PCI4_CLK	CK505_PCI4_CLK - @k2_lib.K2	29B5 30A5 105D3
	TP_CK505_PCI4_CLK - @k2_lib.K2	30A3
CK505_PCI5_CLK_FCTSEL	CK505_PCI5_CLK_FCTSEL - @k2_lib.K2	29B5 30D8 105D3
CK505_PCIF0_CLK_ITPEN	CK505_PCIF0_CLK_ITPEN - @k2_lib.K2	29B7 30A5 105D3
CK505_PCIF1_CLK	CK505_PCIF1_CLK - @k2_lib.K2	29B5 30A5 105D3
CK505_REF0_FSC	CK505_REF0_FSC - @k2_lib.K2	29A3 30A8 105D3
CK505_REF1	CK505_REF1 - @k2_lib.K2	29A3 30B2
	TP_CK505_REF1 - @k2_lib.K2	7C3 30B1
CK505_SRC1_N	CK505_SRC1_N - @k2_lib.K2	29B3 30C5 105C3
	GPU_CLK100M_PCIE_N - @k2_lib.K2	30C3 85C7 105B3
CK505_SRC1_P	CK505_SRC1_P - @k2_lib.K2	29B3 30C5 105C3
	GPU_CLK100M_PCIE_P - @k2_lib.K2	30C3 85C7 105B3
CK505_SRC2_N	CK505_SRC2_N - @k2_lib.K2	29B3 30C5 105C3
	SB_CLK100M_DMI_N - @k2_lib.K2	7B8 7C3 24D2 30C3 105B3
CK505_SRC2_P	CK505_SRC2_P - @k2_lib.K2	29B3 30C5 105C3
	SB_CLK100M_DMI_P - @k2_lib.K2	7B3 7B8 24C2 30C3 105B3

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CK505_SRC3_N	CK505_SRC3_N - @k2_lib.K2	29B3 30C5 105C3
	PCIE_CLK100M_FW_N - @k2_lib.K2	7D6 30C3 40C3 105B3
CK505_SRC3_P	CK505_SRC3_P - @k2_lib.K2	29B3 30C5 105C3
	PCIE_CLK100M_FW_P - @k2_lib.K2	7D6 30C3 40C3 105B3
CK505_SRC4_N	CK505_SRC4_N - @k2_lib.K2	29B3 30B5 105C3
	SB_CLK100M_SATA_N - @k2_lib.K2	7C8 23B6 30B3 105B3
CK505_SRC4_P	CK505_SRC4_P - @k2_lib.K2	29B3 30B5 105C3
	SB_CLK100M_SATA_P - @k2_lib.K2	7C8 23B6 30B3 105B3
CK505_SRC5_N	CK505_SRC5_N - @k2_lib.K2	29B3 30B5 105C3
	NB_CLK100M_PCIE_N - @k2_lib.K2	7C3 7C7 16C3 30B3 105B3
CK505_SRC5_P	CK505_SRC5_P - @k2_lib.K2	29B3 30B5 105C3
	NB_CLK100M_PCIE_P - @k2_lib.K2	7C7 16C3 30B3 105B3
CK505_SRC6_N	CK505_SRC6_N - @k2_lib.K2	29B3 30B5 105C3
	PCIE_CLK100M_MINI_N - @k2_lib.K2	30B3 34C6 105B3
CK505_SRC6_P	CK505_SRC6_P - @k2_lib.K2	29B3 30B5 105C3
	PCIE_CLK100M_MINI_P - @k2_lib.K2	30B3 34C6 105B3
CK505_SRC7_N	CK505_SRC7_N - @k2_lib.K2	29B3 30B5 105C3
CK505_SRC7_P	CK505_SRC7_P - @k2_lib.K2	29B3 30B5 105C3
CK505_SRC8_N	CK505_SRC8_N - @k2_lib.K2	29B3 30B5 105C3
	PCIE_CLK100M_ENET_N - @k2_lib.K2	7D6 30B3 37C8 105B3
CK505_SRC8_P	CK505_SRC8_P - @k2_lib.K2	29A3 30B5 105C3
	PCIE_CLK100M_ENET_P - @k2_lib.K2	7D6 30B3 37C8 105B3
CK505_XTAL_IN	CK505_XTAL_IN - @k2_lib.K2	29C5
CK505_XTAL_OUT	CK505_XTAL_OUT - @k2_lib.K2	29C5
CLINK_NB_CLK	CLINK_NB_CLK - @k2_lib.K2	7A7 7A8 16A3 25C3 104B3
CLINK_NB_DATA	CLINK_NB_DATA - @k2_lib.K2	7A7 7A8 16A3 25C3 104B3
CLINK_NB_RESET_L	CLINK_NB_RESET_L - @k2_lib.K2	16A3 25C3 104B3
CLINK_WLAN_CLK	CLINK_WLAN_CLK - @k2_lib.K2	34A8
	TP_CLINK_WLAN_CLK - @k2_lib.K2	25C3 34A6
CLINK_WLAN_DATA	CLINK_WLAN_DATA - @k2_lib.K2	34A8
	TP_CLINK_WLAN_DATA - @k2_lib.K2	7D2 25C3 28C4 34A6
CLINK_WLAN_RESET_L	CLINK_WLAN_RESET_L - @k2_lib.K2	34A8
	TP_CLINK_WLAN_RESET_L - @k2_lib.K2	25D5 34A6
CLK_PWRGD	CLK_PWRGD - @k2_lib.K2	25C3 29A3
CPUVCORE_ISENSE_CAL	CPUVCORE_ISENSE_CAL - @k2_lib.K2	53B6
CPUVSENSE_IN	CPUVSENSE_IN - @k2_lib.K2	53D7
CPU_A20M_L	CPU_A20M_L - @k2_lib.K2	7C8 10C8 23C4 100B3
CPU_BSEL<0>	CPU_BSEL<0> - @k2_lib.K2	10B4 30C6 100B3
CPU_BSEL<1>	CPU_BSEL<1> - @k2_lib.K2	10A4 30B6 100B3
CPU_BSEL<2>	CPU_BSEL<2> - @k2_lib.K2	10A4 30B6 100A3
CPU_COMP<0>	CPU_COMP<0> - @k2_lib.K2	10B3 100A3
CPU_COMP<1>	CPU_COMP<1> - @k2_lib.K2	10B3 100A3
CPU_COMP<2>	CPU_COMP<2> - @k2_lib.K2	10B3 100A3
CPU_COMP<3>	CPU_COMP<3> - @k2_lib.K2	10B3 100A3
CPU_DPRSTP_L	CPU_DPRSTP_L - @k2_lib.K2	10B2 16B6 23C4 71C7 100A3
CPU_DPSLP_L	CPU_DPSLP_L - @k2_lib.K2	10B2 23C4 100B3
CPU_FERR_L	CPU_FERR_L - @k2_lib.K2	10C8 23C2 100B3
CPU_GTLREF	CPU_GTLREF - @k2_lib.K2	10B4 100A3
CPU_HSK_THRMD_N	CPU_HSK_THRMD_N - @k2_lib.K2	55A5 55A7 108A3
CPU_HSK_THRMD_P	CPU_HSK_THRMD_P - @k2_lib.K2	55A7 55B5 108A3
CPU_IERR_L	CPU_IERR_L - @k2_lib.K2	10D6 100B3
CPU_IGNNE_L	CPU_IGNNE_L - @k2_lib.K2	7C8 10C8 23C4 100B3
CPU_INIT_L	CPU_INIT_L - @k2_lib.K2	7C8 10D6 23C4 51B2 100B3
CPU_INIT_LS3V3	CPU_INIT_LS3V3 - @k2_lib.K2	51C4
CPU_INIT_R_L	CPU_INIT_R_L - @k2_lib.K2	51B3
CPU_INTR	CPU_INTR - @k2_lib.K2	7C8 10B8 23C4 100B3
CPU_NMI	CPU_NMI - @k2_lib.K2	7C8 10B8 23C4 100B3
CPU_PROCHOT_BUF	CPU_PROCHOT_BUF - @k2_lib.K2	50D2
CPU_PROCHOT_L	CPU_PROCHOT_L - @k2_lib.K2	10C5 50D3 55D1 100B3
CPU_PROCHOT_L_R	CPU_PROCHOT_L_R - @k2_lib.K2	50D2
CPU_PSI_L	CPU_PSI_L - @k2_lib.K2	10A2 28B7
	IMVP6_PSI_L - @k2_lib.K2	28B6 71C7
CPU_PWRGD	CPU_PWRGD - @k2_lib.K2	7C4 10B2 13C7 23C4 100B3
CPU_SET_SPEED	CPU_SET_SPEED - @k2_lib.K2	25A7 25B3
CPU_SMI_L	CPU_SMI_L - @k2_lib.K2	7C8 10B8 23C4 100B3
CPU_STPCLK_L	CPU_STPCLK_L - @k2_lib.K2	7C8 10B8 23C4 100B3
CPU_TEST1	CPU_TEST1 - @k2_lib.K2	10B4
CPU_TEST2	CPU_TEST2 - @k2_lib.K2	10B4
CPU_TEST4	CPU_TEST4 - @k2_lib.K2	10B4
CPU_THERMD_N	CPU_THERMD_N - @k2_lib.K2	10C6 55C4 108A3
CPU_THERMD_P	CPU_THERMD_P - @k2_lib.K2	10C6 55C4 108A3
CPU_THERMTRIP_R	CPU_THERMTRIP_R - @k2_lib.K2	23C4
CPU_THRM_ALERT	CPU_THRM_ALERT - @k2_lib.K2	55C3
CPU_THRM_PROCHOT	CPU_THRM_PROCHOT - @k2_lib.K2	55D2
CPU_THRM_THERM	CPU_THRM_THERM - @k2_lib.K2	55C3
CPU_VCCSENSE_N	CPU_VCCSENSE_N - @k2_lib.K2	11A5 71A3 100A3
CPU_VCCSENSE_P	CPU_VCCSENSE_P - @k2_lib.K2	11A5 71A3 100A3
CPU_VID<0>	CPU_VID<0> - @k2_lib.K2	11B6 12C2
CPU_VID<6..0>	CPU_VID<6..0> - @k2_lib.K2	100A3
CPU_VID<1>	CPU_VID<1> - @k2_lib.K2	11B6 12C2
CPU_VID<2>	CPU_VID<2> - @k2_lib.K2	11B6 12C2
CPU_VID<3>	CPU_VID<3> - @k2_lib.K2	11B6 12C2
CPU_VID<4>	CPU_VID<4> - @k2_lib.K2	11B6 12C2
CPU_VID<5>	CPU_VID<5> - @k2_lib.K2	11B6 12C2
CPU_VID<6>	CPU_VID<6> - @k2_lib.K2	11B6 12C2
DEBUG_RESET_L	DEBUG_RESET_L - @k2_lib.K2	7D4 28D1 51B6
DMI_IRCOMP_R	DMI_IRCOMP_R - @k2_lib.K2	24C3
DMI_N2S_N<0>	DMI_N2S_N<0> - @k2_lib.K2	7B8 16B3 24D2
DMI_N2S_N<3..0>	DMI_N2S_N<3..0> - @k2_lib.K2	101D3
DMI_N2S_N<1>	DMI_N2S_N<1> - @k2_lib.K2	16B3 24D2
DMI_N2S_N<2>	DMI_N2S_N<2> - @k2_lib.K2	16B3 24D2
DMI_N2S_N<3>	DMI_N2S_N<3> - @k2_lib.K2	16B3 24D2
DMI_N2S_P<0>	DMI_N2S_P<0> - @k2_lib.K2	7B8 16B3 24D2 101D3
DMI_N2S_P<1>	DMI_N2S_P<1> - @k2_lib.K2	16B3 24D2
DMI_N2S_P<3..1>	DMI_N2S_P<3..1> - @k2_lib.K2	101D3
DMI_N2S_P<2>	DMI_N2S_P<2> - @k2_lib.K2	16B3 24D2
DMI_N2S_P<3>	DMI_N2S_P<3> - @k2_lib.K2	16B3 24D2
DMI_S2N_N<0>	DMI_S2N_N<0> - @k2_lib.K2	7C7 16C3 24D2
DMI_S2N_N<3..0>	DMI_S2N_N<3..0> - @k2_lib.K2	101C3
DMI_S2N_N<1>	DMI_S2N_N<1> - @k2_lib.K2	16C3 24D2
DMI_S2N_N<2>	DMI_S2N_N<2> - @k2_lib.K2	16B3 24D2
DMI_S2N_N<3>	DMI_S2N_N<3> - @k2_lib.K2	16B3 24D2
DMI_S2N_P<0>	DMI_S2N_P<0> - @k2_lib.K2	7C7 16B3 24D2 101C3
DMI_S2N_P<1>	DMI_S2N_P<1> - @k2_lib.K2	16B3 24D2
DMI_S2N_P<3..1>	DMI_S2N_P<3..1> - @k2_lib.K2	101D3
DMI_S2N_P<2>	DMI_S2N_P<2> - @k2_lib.K2	16B3 24D2
DMI_S2N_P<3>	DMI_S2N_P<3> - @k2_lib.K2	16B3 24D2
DVI_DDC_CLK	DVI_DDC_CLK - @k2_lib.K2	94D2
DVI_DDC_CLK_UF	DVI_DDC_CLK_UF - @k2_lib.K2	94D3 94D5
DVI_DDC_DATA	DVI_DDC_DATA - @k2_lib.K2	94C2
DVI_DDC_DATA_UF	DVI_DDC_DATA_UF - @k2_lib.K2	94C3 94D5
DVI_HOTPLUG_DET	DVI_HOTPLUG_DET - @k2_lib.K2	24A6 28B2
	SB_GPIO4 - @k2_lib.K2	28B2
DVI_HPD_UF	DVI_HPD_UF - @k2_lib.K2	94C3 94D5
ENET_CLK25M_XTALI	ENET_CLK25M_XTALI - @k2_lib.K2	7B3 37B4
ENET_CLK25M_XTALO	ENET_CLK25M_XTALO - @k2_lib.K2	7B3 37B4
ENET_CTAP_<0>	ENET_CTAP_<0> - @k2_lib.K2	39B5
ENET_CTAP_<1>	ENET_CTAP_<1> - @k2_lib.K2	39B5
ENET_CTAP_<2>	ENET_CTAP_<2> - @k2_lib.K2	39B5
ENET_CTAP_<3>	ENET_CTAP_<3> - @k2_lib.K2	39B5
ENET_CTAP_COMMON	ENET_CTAP_COMMON - @k2_lib.K2	39A4
ENET_CTRL12	ENET_CTRL12 - @k2_lib.K2	38A5 38B1
	TP_YUKON_CTRL12 - @k2_lib.K2	37C2 38B3
ENET_CTRL19	ENET_CTRL19 - @k2_lib.K2	38B1 38C5

	TP_YUKON_CTRL18 - @k2_lib.K2	37C2 38B3
ENET_LED_ACT_L	ENET_LED_ACT_L - @k2_lib.K2	37B2 39A8
ENET_LED_LINK10_100_L	ENET_LED_LINK10_100_L - @k2_lib.K2	37B2 39A8
ENET_LED_LINK1000_L	ENET_LED_LINK1000_L - @k2_lib.K2	37B2 39A8
ENET_LED_LINK_L	ENET_LED_LINK_L - @k2_lib.K2	37B2 39A8
ENET_LOM_DIS_L	ENET_LOM_DIS_L - @k2_lib.K2	37C2
ENET_MDI0	ENET_MDI0 - @k2_lib.K2	37B7 104B3
ENET_MDI1	ENET_MDI1 - @k2_lib.K2	37B6 104B3
ENET_MDI2	ENET_MDI2 - @k2_lib.K2	37B6 104B3
ENET_MDI3	ENET_MDI3 - @k2_lib.K2	37B5 104B3
ENET_MDI_N<0>	ENET_MDI_N<0> - @k2_lib.K2	37B8 39C7 104B3
ENET_MDI_N<1>	ENET_MDI_N<1> - @k2_lib.K2	37B8 39C7 104B3
ENET_MDI_N<2>	ENET_MDI_N<2> - @k2_lib.K2	37B8 39B7 104A3
ENET_MDI_N<3>	ENET_MDI_N<3> - @k2_lib.K2	37B8 39B7 104A3
ENET_MDI_P<0>	ENET_MDI_P<0> - @k2_lib.K2	37B8 39C7 104B3
ENET_MDI_P<1>	ENET_MDI_P<1> - @k2_lib.K2	37B8 39C7 104B3
ENET_MDI_P<2>	ENET_MDI_P<2> - @k2_lib.K2	37B8 39B7 104B3
ENET_MDI_P<3>	ENET_MDI_P<3> - @k2_lib.K2	37B8 39B7 104A3
ENET_MDI_R_N<0>	ENET_MDI_R_N<0> - @k2_lib.K2	108B3
ENET_MDI_R_N<1>	ENET_MDI_R_N<1> - @k2_lib.K2	108B3
ENET_MDI_R_N<2>	ENET_MDI_R_N<2> - @k2_lib.K2	108B3
ENET_MDI_R_N<3>	ENET_MDI_R_N<3> - @k2_lib.K2	108B3
ENET_MDI_R_P<0>	ENET_MDI_R_P<0> - @k2_lib.K2	108B3
ENET_MDI_R_P<1>	ENET_MDI_R_P<1> - @k2_lib.K2	108B3
ENET_MDI_R_P<2>	ENET_MDI_R_P<2> - @k2_lib.K2	108B3
ENET_MDI_R_P<3>	ENET_MDI_R_P<3> - @k2_lib.K2	108B3
ENET_MDI_T_N<0>	ENET_MDI_T_N<0> - @k2_lib.K2	39C5 108B3
ENET_MDI_T_N<1>	ENET_MDI_T_N<1> - @k2_lib.K2	39C5 108B3
ENET_MDI_T_N<2>	ENET_MDI_T_N<2> - @k2_lib.K2	39B5 108B3
ENET_MDI_T_N<3>	ENET_MDI_T_N<3> - @k2_lib.K2	39B5 108B3
ENET_MDI_T_P<0>	ENET_MDI_T_P<0> - @k2_lib.K2	39C5 108B3
ENET_MDI_T_P<1>	ENET_MDI_T_P<1> - @k2_lib.K2	39C5 108B3
ENET_MDI_T_P<2>	ENET_MDI_T_P<2> - @k2_lib.K2	39B5 108B3
ENET_MDI_T_P<3>	ENET_MDI_T_P<3> - @k2_lib.K2	39B5 108B3
ENET_RESET_L	ENET_RESET_L - @k2_lib.K2	7D6 28C1 37B8
EXCARD_OC_L	EXCARD_OC_L - @k2_lib.K2	24C8
EXTGPU_LVDS_EN	EXTGPU_LVDS_EN - @k2_lib.K2	13C3 24C8
EXTGPU_PWR_EN	EXTGPU_PWR_EN - @k2_lib.K2	23C4 28A2
	TP_EXTGPU_PWR_EN - @k2_lib.K2	28A1
EXTGPU_RST_L	EXTGPU_RST_L - @k2_lib.K2	25A5 25C5 28A2
	TP_EXTGPU_RST_L - @k2_lib.K2	28A1
F0_GATESLOWDN	F0_GATESLOWDN - @k2_lib.K2	56D5
F0_VOLTAGE8R5	F0_VOLTAGE8R5 - @k2_lib.K2	56D6
F1_GATESLOWDN	F1_GATESLOWDN - @k2_lib.K2	56B5
F1_VOLTAGE8R5	F1_VOLTAGE8R5 - @k2_lib.K2	56B6
F2_GATESLOWDN	F2_GATESLOWDN - @k2_lib.K2	57D4
F2_VOLTAGE8R5	F2_VOLTAGE8R5 - @k2_lib.K2	57D5
FAN_0_PWR	FAN_0_PWR - @k2_lib.K2	56C4
FAN_1_PWR	FAN_1_PWR - @k2_lib.K2	56B3
FAN_2_PWR	FAN_2_PWR - @k2_lib.K2	57C3
FAN_TACH0	FAN_TACH0 - @k2_lib.K2	56C7
FAN_TACH1	FAN_TACH1 - @k2_lib.K2	56A7
FAN_TACH2	FAN_TACH2 - @k2_lib.K2	57C7
FSB_ADSTB_L<0>	FSB_ADSTB_L<0> - @k2_lib.K2	7D7 7D8 10D8 14C3 100C3
FSB_ADSTB_L<1>	FSB_ADSTB_L<1> - @k2_lib.K2	7D7 7D8 10C8 14C3 100B3
FSB_ADS_L	FSB_ADS_L - @k2_lib.K2	10D6 14C3 100D3
FSB_A_L<3>	FSB_A_L<3> - @k2_lib.K2	10D8 14D3
FSB_A_L<5..3>	FSB_A_L<5..3> - @k2_lib.K2	100C3
FSB_A_L<4>	FSB_A_L<4> - @k2_lib.K2	10D8 14D3
FSB_A_L<5>	FSB_A_L<5> - @k2_lib.K2	10D8 14D3
FSB_A_L<6>	FSB_A_L<6> - @k2_lib.K2	7D7 7D8 10D8 14D3 100C3
FSB_A_L<7>	FSB_A_L<7> - @k2_lib.K2	10D8 14D3
FSB_A_L<16..7>	FSB_A_L<16..7> - @k2_lib.K2	100C3
FSB_A_L<8>	FSB_A_L<8> - @k2_lib.K2	10D8 14D3
FSB_A_L<9>	FSB_A_L<9> - @k2_lib.K2	10D8 14D3
FSB_A_L<10>	FSB_A_L<10> - @k2_lib.K2	10D8 14D3
FSB_A_L<11>	FSB_A_L<11> - @k2_lib.K2	10D8 14D3
FSB_A_L<12>	FSB_A_L<12> - @k2_lib.K2	10D8 14D3
FSB_A_L<13>	FSB_A_L<13> - @k2_lib.K2	10D8 14D3
FSB_A_L<14>	FSB_A_L<14> - @k2_lib.K2	10D8 14D3
FSB_A_L<15>	FSB_A_L<15> - @k2_lib.K2	10D8 14D3
FSB_A_L<16>	FSB_A_L<16> - @k2_lib.K2	10D8 14C3
FSB_A_L<17>	FSB_A_L<17> - @k2_lib.K2	10C8 14C3
FSB_A_L<26..17>	FSB_A_L<26..17> - @k2_lib.K2	100B3
FSB_A_L<18>	FSB_A_L<18> - @k2_lib.K2	10C8 14C3
FSB_A_L<19>	FSB_A_L<19> - @k2_lib.K2	10C8 14C3
FSB_A_L<20>	FSB_A_L<20> - @k2_lib.K2	10C8 14C3
FSB_A_L<21>	FSB_A_L<21> - @k2_lib.K2	10C8 14C3
FSB_A_L<22>	FSB_A_L<22> - @k2_lib.K2	10C8 14C3
FSB_A_L<23>	FSB_A_L<23> - @k2_lib.K2	10C8 14C3
FSB_A_L<24>	FSB_A_L<24> - @k2_lib.K2	10C8 14C3
FSB_A_L<25>	FSB_A_L<25> - @k2_lib.K2	10C8 14C3
FSB_A_L<26>	FSB_A_L<26> - @k2_lib.K2	10C8 14C3
FSB_A_L<27>	FSB_A_L<27> - @k2_lib.K2	7D7 7D8 10C8 14C3 100B3
FSB_A_L<28>	FSB_A_L<28> - @k2_lib.K2	10C8 14C3
FSB_A_L<35..28>	FSB_A_L<35..28> - @k2_lib.K2	100B3
FSB_A_L<29>	FSB_A_L<29> - @k2_lib.K2	10C8 14C3
FSB_A_L<30>	FSB_A_L<30> - @k2_lib.K2	10C8 14C3
FSB_A_L<31>	FSB_A_L<31> - @k2_lib.K2	10C8 14C3
FSB_A_L<32>	FSB_A_L<32> - @k2_lib.K2	10C8 14C3
FSB_A_L<33>	FSB_A_L<33> - @k2_lib.K2	10C8 14C3
FSB_A_L<34>	FSB_A_L<34> - @k2_lib.K2	10C8 14C3
FSB_A_L<35>	FSB_A_L<35> - @k2_lib.K2	10C8 14C3
FSB_BNR_L	FSB_BNR_L - @k2_lib.K2	7C7 10D6 14C3 100D3
FSB_BPRI_L	FSB_BPRI_L - @k2_lib.K2	10D6 14C3 100D3
FSB_BREQ0_L	FSB_BREQ0_L - @k2_lib.K2	7C7 10D6 14B3 100D3
FSB_CPURST_L	FSB_CPURST_L - @k2_lib.K2	7C8 10D6 13B2 14A5 100D3
FSB_CPUSLP_L	FSB_CPUSLP_L - @k2_lib.K2	10A2 14A5 100B3
FSB_DBSY_L	FSB_DBSY_L - @k2_lib.K2	7C7 10D6 14B3 100D3
FSB_DEFER_L	FSB_DEFER_L - @k2_lib.K2	10D6 14B3 100D3
FSB_DINV_L<0>	FSB_DINV_L<0> - @k2_lib.K2	7D7 7D8 10C4 14B3 100D3
FSB_DINV_L<1>	FSB_DINV_L<1> - @k2_lib.K2	7D7 7D8 10B4 14B3 100C3
FSB_DINV_L<2>	FSB_DINV_L<2> - @k2_lib.K2	7D7 7D8 10C2 14B3 100C3
FSB_DINV_L<3>	FSB_DINV_L<3> - @k2_lib.K2	7D7 7D8 10B2 14B3 100C3
FSB_DPWR_L	FSB_DPWR_L - @k2_lib.K2	7C7 10B2 14B3 100D3
FSB_DRDY_L	FSB_DRDY_L - @k2_lib.K2	10D6 14B3 100D3
FSB_DSTB_L_N<0>	FSB_DSTB_L_N<0> - @k2_lib.K2	7D7 7D8 10C4 14B3 100C3
FSB_DSTB_L_N<1>	FSB_DSTB_L_N<1> - @k2_lib.K2	7D7 7D8 10B4 14B3 100C3
FSB_DSTB_L_N<2>	FSB_DSTB_L_N<2> - @k2_lib.K2	7D7 7D8 10C2 14B3 100C3
FSB_DSTB_L_N<3>	FSB_DSTB_L_N<3> - @k2_lib.K2	7D7 7D8 10B2 14B3 100C3
FSB_DSTB_L_P<0>	FSB_DSTB_L_P<0> - @k2_lib.K2	7D7 7D8 10C4 14B3 100D3
FSB_DSTB_L_P<1>	FSB_DSTB_L_P<1> - @k2_lib.K2	7D7 7D8 10B4 14B3 100C3
FSB_DSTB_L_P<2>	FSB_DSTB_L_P<2> - @k2_lib.K2	7D7 7D8 10C2 14A3 100C3
FSB_DSTB_L_P<3>	FSB_DSTB_L_P<3> - @k2_lib.K2	7D7 7D8 10B2 14A3 100C3
FSB_D_L<0>	FSB_D_L<0> - @k2_lib.K2	7D7 7D8 10C4 14D5 100D3
FSB_D_L<1>	FSB_D_L<1> - @k2_lib.K2	10C4 14D5
FSB_D_L<15..1>	FSB_D_L<15..1> - @k2_lib.K2	100D3
FSB_D_L<2>	FSB_D_L<2> - @k2_lib.K2	10C4 14D5
FSB_D_L<3>	FSB_D_L<3> - @k2_lib.K2	10C4 14D5
FSB_D_L<4>	FSB_D_L<4> - @k2_lib.K2	10C4 14D5
FSB_D_L<5>	FSB_D_L<5> - @k2_lib.K2	10C4 14D5
FSB_D_L<6>	FSB_D_L<6> - @k2_lib.K2	10C4 14D5
FSB_D_L<7>	FSB_D_L<7> - @k2_lib.K2	10C4 14D5

FSB_D_L<8>	FSB_D_L<8> - @k2_lib.K2	10C4 14D5
FSB_D_L<9>	FSB_D_L<9> - @k2_lib.K2	10C4 14D5
FSB_D_L<10>	FSB_D_L<10> - @k2_lib.K2	10C4 14D5
FSB_D_L<11>	FSB_D_L<11> - @k2_lib.K2	10C4 14D5
FSB_D_L<12>	FSB_D_L<12> - @k2_lib.K2	10C4 14D5
FSB_D_L<13>	FSB_D_L<13> - @k2_lib.K2	10C4 14C5
FSB_D_L<14>	FSB_D_L<14> - @k2_lib.K2	10C4 14C5
FSB_D_L<15>	FSB_D_L<15> - @k2_lib.K2	10C4 14C5
FSB_D_L<16>	FSB_D_L<16> - @k2_lib.K2	7D7 7D8 10C4 14C5 100C3
FSB_D_L<17>	FSB_D_L<17> - @k2_lib.K2	10C4 14C5
FSB_D_L<31..17>	FSB_D_L<31..17> - @k2_lib.K2	100C3
FSB_D_L<18>	FSB_D_L<18> - @k2_lib.K2	10C4 14C5
FSB_D_L<19>	FSB_D_L<19> - @k2_lib.K2	10B4 14C5
FSB_D_L<20>	FSB_D_L<20> - @k2_lib.K2	10B4 14C5
FSB_D_L<21>	FSB_D_L<21> - @k2_lib.K2	10B4 14C5
FSB_D_L<22>	FSB_D_L<22> - @k2_lib.K2	10B4 14C5
FSB_D_L<23>	FSB_D_L<23> - @k2_lib.K2	10B4 14C5
FSB_D_L<24>	FSB_D_L<24> - @k2_lib.K2	10B4 14C5
FSB_D_L<25>	FSB_D_L<25> - @k2_lib.K2	10B4 14C5
FSB_D_L<26>	FSB_D_L<26> - @k2_lib.K2	10B4 14C5
FSB_D_L<27>	FSB_D_L<27> - @k2_lib.K2	10B4 14C5
FSB_D_L<28>	FSB_D_L<28> - @k2_lib.K2	10B4 14C5
FSB_D_L<29>	FSB_D_L<29> - @k2_lib.K2	10B4 14C5
FSB_D_L<30>	FSB_D_L<30> - @k2_lib.K2	10B4 14C5
FSB_D_L<31>	FSB_D_L<31> - @k2_lib.K2	10B4 14C5
FSB_D_L<32>	FSB_D_L<32> - @k2_lib.K2	10C2 14C5
FSB_D_L<40..32>	FSB_D_L<40..32> - @k2_lib.K2	100C3
FSB_D_L<33>	FSB_D_L<33> - @k2_lib.K2	10C2 14C5
FSB_D_L<34>	FSB_D_L<34> - @k2_lib.K2	10C2 14C5
FSB_D_L<35>	FSB_D_L<35> - @k2_lib.K2	10C2 14C5
FSB_D_L<36>	FSB_D_L<36> - @k2_lib.K2	10C2 14C5
FSB_D_L<37>	FSB_D_L<37> - @k2_lib.K2	10C2 14C5
FSB_D_L<38>	FSB_D_L<38> - @k2_lib.K2	10C2 14C5
FSB_D_L<39>	FSB_D_L<39> - @k2_lib.K2	10C2 14B5
FSB_D_L<40>	FSB_D_L<40> - @k2_lib.K2	10C2 14B5
FSB_D_L<41>	FSB_D_L<41> - @k2_lib.K2	7D7 7D8 10C2 14B5 100C3
FSB_D_L<42>	FSB_D_L<42> - @k2_lib.K2	10C2 14B5
FSB_D_L<47..42>	FSB_D_L<47..42> - @k2_lib.K2	100C3
FSB_D_L<43>	FSB_D_L<43> - @k2_lib.K2	10C2 14B5
FSB_D_L<44>	FSB_D_L<44> - @k2_lib.K2	10C2 14B5
FSB_D_L<45>	FSB_D_L<45> - @k2_lib.K2	10C2 14B5
FSB_D_L<46>	FSB_D_L<46> - @k2_lib.K2	10C2 14B5
FSB_D_L<47>	FSB_D_L<47> - @k2_lib.K2	10C2 14B5
FSB_D_L<48>	FSB_D_L<48> - @k2_lib.K2	10C2 14B5
FSB_D_L<58..48>	FSB_D_L<58..48> - @k2_lib.K2	100C3
FSB_D_L<49>	FSB_D_L<49> - @k2_lib.K2	10C2 14B5
FSB_D_L<50>	FSB_D_L<50> - @k2_lib.K2	10C2 14B5
FSB_D_L<51>	FSB_D_L<51> - @k2_lib.K2	10B2 14B5
FSB_D_L<52>	FSB_D_L<52> - @k2_lib.K2	10B2 14B5
FSB_D_L<53>	FSB_D_L<53> - @k2_lib.K2	10B2 14B5
FSB_D_L<54>	FSB_D_L<54> - @k2_lib.K2	10B2 14B5
FSB_D_L<55>	FSB_D_L<55> - @k2_lib.K2	10B2 14B5
FSB_D_L<56>	FSB_D_L<56> - @k2_lib.K2	10B2 14B5
FSB_D_L<57>	FSB_D_L<57> - @k2_lib.K2	10B2 14B5
FSB_D_L<58>	FSB_D_L<58> - @k2_lib.K2	10B2 14B5
FSB_D_L<59>	FSB_D_L<59> - @k2_lib.K2	7D7 7D8 10B2 14B5 100C3
FSB_D_L<60>	FSB_D_L<60> - @k2_lib.K2	10B2 14B5
FSB_D_L<63..60>	FSB_D_L<63..60> - @k2_lib.K2	100C3
FSB_D_L<61>	FSB_D_L<61> - @k2_lib.K2	10B2 14B5
FSB_D_L<62>	FSB_D_L<62> - @k2_lib.K2	10B2 14B5
FSB_D_L<63>	FSB_D_L<63> - @k2_lib.K2	10B2 14B5
FSB_HITM_L	FSB_HITM_L - @k2_lib.K2	7C7 10C6 14B3 100D3
FSB_HIT_L	FSB_HIT_L - @k2_lib.K2	7C7 10C6 14B3 100D3
FSB_LOCK_L	FSB_LOCK_L - @k2_lib.K2	7D7 7D8 10D6 14B3 100D3
FSB_REQ_L<0>	FSB_REQ_L<0> - @k2_lib.K2	7C7 7C8 10D8 14A3
FSB_REQ_L<4..0>	FSB_REQ_L<4..0> - @k2_lib.K2	100C3
FSB_REQ_L<1>	FSB_REQ_L<1> - @k2_lib.K2	7C7 7C8 10D8 14A3
FSB_REQ_L<2>	FSB_REQ_L<2> - @k2_lib.K2	7C7 7C8 10D8 14A3
FSB_REQ_L<3>	FSB_REQ_L<3> - @k2_lib.K2	7C7 7C8 10D8 14A3
FSB_REQ_L<4>	FSB_REQ_L<4> - @k2_lib.K2	7C7 7C8 10C8 14A3
FSB_RS_L<0>	FSB_RS_L<0> - @k2_lib.K2	10D6 14A3
FSB_RS_L<2..0>	FSB_RS_L<2..0> - @k2_lib.K2	100D3
FSB_RS_L<1>	FSB_RS_L<1> - @k2_lib.K2	10D6 14A3
FSB_RS_L<2>	FSB_RS_L<2> - @k2_lib.K2	10D6 14A3
FSB_TRDY_L	FSB_TRDY_L - @k2_lib.K2	10D6 14B3 100D3
FW643_REGCTL	FW643_REGCTL - @k2_lib.K2	40C3
FWH_INIT_L	FWH_INIT_L - @k2_lib.K2	7D4 51C5
FWH_MFG_MODE	FWH_MFG_MODE - @k2_lib.K2	25A7 25C5
FW_OCR10_CTL	FW_OCR10_CTL - @k2_lib.K2	40B6 42C8
FW_OCR10_CTL_R	FW_OCR10_CTL_R - @k2_lib.K2	42C7
FW_P0_TPA_C	FW_P0_TPA_C - @k2_lib.K2	43B8
FW_P0_TPBIAS	FW_P0_TPBIAS - @k2_lib.K2	40C6 43D8
FW_P1_TPA_C	FW_P1_TPA_C - @k2_lib.K2	43B7
FW_P1_TPBIAS	FW_P1_TPBIAS - @k2_lib.K2	40C6 43D8
FW_P2_TPA_N	FW_P2_TPA_N - @k2_lib.K2	40C6 43A8
	NC_FW_PORT2_TPA_N - @k2_lib.K2	43A6
FW_P2_TPA_P	FW_P2_TPA_P - @k2_lib.K2	40C6 43A8
	NC_FW_PORT2_TPA_P - @k2_lib.K2	43A6
FW_P2_TPBIAS	FW_P2_TPBIAS - @k2_lib.K2	40C6 43A8
	NC_FW_PORT2_TPBIAS - @k2_lib.K2	43A6
FW_P2_TPB_N	FW_P2_TPB_N - @k2_lib.K2	40C6 43A8
	NC_FW_PORT2_TPB_N - @k2_lib.K2	43A6
FW_P2_TPB_P	FW_P2_TPB_P - @k2_lib.K2	40C6 43A8
	NC_FW_PORT2_TPB_P - @k2_lib.K2	43A6
FW_PHY_DS0	FW_PHY_DS0 - @k2_lib.K2	40C6 42D3
FW_PHY_DS1	FW_PHY_DS1 - @k2_lib.K2	40C6 42D3
FW_PHY_DS2	FW_PHY_DS2 - @k2_lib.K2	40C6 42D3
FW_PORT0_TPA_N	FW_PORT0_TPA_N - @k2_lib.K2	43C5 43C6 106D3
	FW_P0_TPA_N - @k2_lib.K2	40C6 43C8
FW_PORT0_TPA_P	FW_PORT0_TPA_P - @k2_lib.K2	43C5 43C6 106D3
	FW_P0_TPA_P - @k2_lib.K2	40C6 43C8
FW_PORT0_TPA_R	FW_PORT0_TPA_R - @k2_lib.K2	43C2
FW_PORT0_TPB_N	FW_PORT0_TPB_N - @k2_lib.K2	43C5 43C6 106D3
	FW_P0_TPB_N - @k2_lib.K2	40C6 43C8
FW_PORT0_TPB_P	FW_PORT0_TPB_P - @k2_lib.K2	43C5 43C6 106D3
	FW_P0_TPB_P - @k2_lib.K2	40C6 43C8
FW_PORT0_VP	FW_PORT0_VP - @k2_lib.K2	43D3
FW_PORT0_VP_F	FW_PORT0_VP_F - @k2_lib.K2	43D5
FW_PORT1_TPA_FL_N	FW_PORT1_TPA_FL_N - @k2_lib.K2	43B2 106D3
FW_PORT1_TPA_FL_P	FW_PORT1_TPA_FL_P - @k2_lib.K2	43B2 106D3
FW_PORT1_TPA_N	FW_PORT1_TPA_N - @k2_lib.K2	43B6 43C6 106D3
	FW_P1_TPA_N - @k2_lib.K2	40C6 43C8
FW_PORT1_TPA_P	FW_PORT1_TPA_P - @k2_lib.K2	43B6 43C6 106D3
	FW_P1_TPA_P - @k2_lib.K2	40C6 43C8
FW_PORT1_TPB_FL_N	FW_PORT1_TPB_FL_N - @k2_lib.K2	43B2 106D3
FW_PORT1_TPB_FL_P	FW_PORT1_TPB_FL_P - @k2_lib.K2	43B2 106D3
FW_PORT1_TPB_N	FW_PORT1_TPB_N - @k2_lib.K2	43A6 43C6 106D3
	FW_P1_TPB_N - @k2_lib.K2	40C6 43C8
FW_PORT1_TPB_P	FW_PORT1_TPB_P - @k2_lib.K2	43B6 43C6 106D3
	FW_P1_TPB_P - @k2_lib.K2	40C6 43C8
FW_PORT1_VP	FW_PORT1_VP - @k2_lib.K2	43B3
FW_PORT1_VP_F	FW_PORT1_VP_F - @k2_lib.K2	43D5
FW_PORTS_VP	FW_PORTS_VP - @k2_lib.K2	43D7
FW_PORTS_VP_R	FW_PORTS_VP_R - @k2_lib.K2	40C7 43D6

FW_PU_RST_L	FW_PU_RST_L - @k2_lib.K2	40B6
FW_R0	FW_R0 - @k2_lib.K2	40B6
FW_RESET_L	FW_RESET_L - @k2_lib.K2	7B3 7D6 28C1 40B3
FW_REXT	FW_REXT - @k2_lib.K2	40B6
FW_SCL	FW_SCL - @k2_lib.K2	40B3
FW_TPCPS	FW_TPCPS - @k2_lib.K2	40B6
FW_TRST_L	FW_TRST_L - @k2_lib.K2	7C3 40C3
FW_VAUX_DETECT	FW_VAUX_DETECT - @k2_lib.K2	40C3
FW_XI	FW_XI - @k2_lib.K2	40B6
FW_XO	FW_XO - @k2_lib.K2	40B6
FW_XO_R	FW_XO_R - @k2_lib.K2	40B7
GFX_VID<1>	GFX_VID<1> - @k2_lib.K2	16B3 22B8
GFX_VID<2>	GFX_VID<2> - @k2_lib.K2	16B3 22A8
GFX_VID<3>	GFX_VID<3> - @k2_lib.K2	16B3 22A8
GFX_VID<4>	GFX_VID<4> - @k2_lib.K2	16B3 22A8
GLAN_COMP	GLAN_COMP - @k2_lib.K2	23C6 104B3
GND_IMVP6_SGND	GND_IMVP6_SGND - @k2_lib.K2	71B6
GND_PP1V5REG_SGND	GND_PP1V5REG_SGND - @k2_lib.K2	73B7
GND_PP1V8REG_SGND	GND_PP1V8REG_SGND - @k2_lib.K2	75C5 75D6
GND_PP1V25REG_SGND	GND_PP1V25REG_SGND - @k2_lib.K2	74B7
GND_PP5VREG_SGND	GND_PP5VREG_SGND - @k2_lib.K2	76A7
GND_SMC_AVSS	GND_SMC_AVSS - @k2_lib.K2	49B2 50B7 53A2 53A3 53B1 53C3 53C6 53D3 53D6
GPU_BLU	GPU_BLU - @k2_lib.K2	85C4 91B8 108B3
GPU_BUF_HSYNC	GPU_BUF_HSYNC - @k2_lib.K2	108A3
GPU_BUF_VSYNC	GPU_BUF_VSYNC - @k2_lib.K2	108A3
GPU_DDC_A_CLK	GPU_DDC_A_CLK - @k2_lib.K2	85C7 94D1
GPU_DDC_A_DATA	GPU_DDC_A_DATA - @k2_lib.K2	85C7 94C1
GPU_DDC_C_CLK	GPU_DDC_C_CLK - @k2_lib.K2	85A4 85D1 90A8
GPU_DDC_C_DATA	GPU_DDC_C_DATA - @k2_lib.K2	85A4 85D1 90A6
GPU_DIGON	GPU_DIGON - @k2_lib.K2	85A4 90B8
GPU_ENABLE_BL	GPU_ENABLE_BL - @k2_lib.K2	85A5
GPU_GRN	GPU_GRN - @k2_lib.K2	85C4 91B8 108B3
GPU_H2SYNC	GPU_H2SYNC - @k2_lib.K2	85C7 91A4 108B3
GPU_HPD	GPU_HPD - @k2_lib.K2	85A7 94C1
GPU_HSK_THRMD_N	GPU_HSK_THRMD_N - @k2_lib.K2	55A5 55A6 108A3
GPU_HSK_THRMD_P	GPU_HSK_THRMD_P - @k2_lib.K2	55A6 55B5 108A3
GPU_HSYNC_BUF	GPU_HSYNC_BUF - @k2_lib.K2	91A3
GPU_PRESENT	GPU_PRESENT - @k2_lib.K2	6A8 28C1
	SB_GPIO6 - @k2_lib.K2	25A5 25C5 28C2
GPU_PRESENT_DRAIN	GPU_PRESENT_DRAIN - @k2_lib.K2	6B7
GPU_PRESENT_R	GPU_PRESENT_R - @k2_lib.K2	6B7
GPU_RED	GPU_RED - @k2_lib.K2	85C4 91B8 108B3
GPU_TV_C	GPU_TV_C - @k2_lib.K2	85C4 91B8 108B3
GPU_TV_COMP	GPU_TV_COMP - @k2_lib.K2	85C4 91B8 108B3
GPU_TV_Y	GPU_TV_Y - @k2_lib.K2	85C4 91B8 108B3
GPU_V2SYNC	GPU_V2SYNC - @k2_lib.K2	85C7 91B4 108A3
GPU_VARY_BL	GPU_VARY_BL - @k2_lib.K2	85A4 90B3
GPU_VSYNC_BUF	GPU_VSYNC_BUF - @k2_lib.K2	91B3
HDA_BIT_CLK	HDA_BIT_CLK - @k2_lib.K2	23C8 98C6 103C3
HDA_BIT_CLK_R	HDA_BIT_CLK_R - @k2_lib.K2	23C6 103C3
HDA_DOCK_EN_L	HDA_DOCK_EN_L - @k2_lib.K2	23B6
HDA_RST_L	HDA_RST_L - @k2_lib.K2	23C8 98C6 103C3
HDA_RST_L_R	HDA_RST_L_R - @k2_lib.K2	23C6 103C3
HDA_SDIN0	HDA_SDIN0 - @k2_lib.K2	23C8 98C6 103B3
HDA_SDIN_CODEC	HDA_SDIN_CODEC - @k2_lib.K2	103B3
HDA_SDOUT	HDA_SDOUT - @k2_lib.K2	23B8 98C6 103B3
HDA_SDOUT_R	HDA_SDOUT_R - @k2_lib.K2	23B6 103B3
HDA_SYNC	HDA_SYNC - @k2_lib.K2	23C8 98C6 103C3
HDA_SYNC_R	HDA_SYNC_R - @k2_lib.K2	23C6 103C3
HDD_THRMD_N	HDD_THRMD_N - @k2_lib.K2	55A5 55B7 108A3
HDD_THRMD_P	HDD_THRMD_P - @k2_lib.K2	55B5 55B7 108A3
IDE_CSEL	IDE_CSEL - @k2_lib.K2	44B5
IDE_DASP_L	IDE_DASP_L - @k2_lib.K2	44B5
IDE_DASP_L_DS	IDE_DASP_L_DS - @k2_lib.K2	44B6
IDE_IOCS16_PU	IDE_IOCS16_PU - @k2_lib.K2	44C3
IDE_IRQ14	IDE_IRQ14 - @k2_lib.K2	23B4 44C6 103D3
IDE_PDA<0>	IDE_PDA<0> - @k2_lib.K2	23B4 44B5
IDE_PDA<2..0>	IDE_PDA<2..0> - @k2_lib.K2	103D3
IDE_PDA<1>	IDE_PDA<1> - @k2_lib.K2	23B4 44B5
IDE_PDA<2>	IDE_PDA<2> - @k2_lib.K2	23B4 44B3
IDE_PDCS1_L	IDE_PDCS1_L - @k2_lib.K2	23B4 44B5 103D3
IDE_PDCS3_L	IDE_PDCS3_L - @k2_lib.K2	23B4 44B3 103D3
IDE_PDD<0>	IDE_PDD<0> - @k2_lib.K2	23C4 44C5
IDE_PDD<8..0>	IDE_PDD<8..0> - @k2_lib.K2	103D3
IDE_PDD<1>	IDE_PDD<1> - @k2_lib.K2	23C4 44C5
IDE_PDD<2>	IDE_PDD<2> - @k2_lib.K2	23B4 44C5
IDE_PDD<3>	IDE_PDD<3> - @k2_lib.K2	23B4 44C5
IDE_PDD<4>	IDE_PDD<4> - @k2_lib.K2	23B4 44C5
IDE_PDD<5>	IDE_PDD<5> - @k2_lib.K2	23B4 44C5
IDE_PDD<6>	IDE_PDD<6> - @k2_lib.K2	23B4 44C5
IDE_PDD<7>	IDE_PDD<7> - @k2_lib.K2	23B4 44C5
IDE_PDD<8>	IDE_PDD<8> - @k2_lib.K2	23B4 44C3
IDE_PDD<9>	IDE_PDD<9> - @k2_lib.K2	7B8 23B4 44C3 103D3
IDE_PDD<10>	IDE_PDD<10> - @k2_lib.K2	23B4 44C3
IDE_PDD<15..10>	IDE_PDD<15..10> - @k2_lib.K2	103D3
IDE_PDD<11>	IDE_PDD<11> - @k2_lib.K2	23B4 44C3
IDE_PDD<12>	IDE_PDD<12> - @k2_lib.K2	23B4 44C3
IDE_PDD<13>	IDE_PDD<13> - @k2_lib.K2	23B4 44C3
IDE_PDD<14>	IDE_PDD<14> - @k2_lib.K2	23B4 44C3
IDE_PDD<15>	IDE_PDD<15> - @k2_lib.K2	23B4 44C3
IDE_PDDACK_L	IDE_PDDACK_L - @k2_lib.K2	23B4 44C3 103D3
IDE_PDDREQ	IDE_PDDREQ - @k2_lib.K2	23A4 44B6 103D3
IDE_PDIORDY	IDE_PDIORDY - @k2_lib.K2	7B8 23A4 44C6 103D3
IDE_PDIOR_L	IDE_PDIOR_L - @k2_lib.K2	7C8 23B4 44C3 103D3
IDE_PDIOW_L	IDE_PDIOW_L - @k2_lib.K2	23B4 44C5 103D3
IMVP6_BOOT1	IMVP6_BOOT1 - @k2_lib.K2	71A6 71D4
IMVP6_BOOT1_RC	IMVP6_BOOT1_RC - @k2_lib.K2	71A6 71D4
IMVP6_BOOT2	IMVP6_BOOT2 - @k2_lib.K2	71A4 71C4
IMVP6_BOOT2_RC	IMVP6_BOOT2_RC - @k2_lib.K2	71A4 71C4
IMVP6_BOOT3	IMVP6_BOOT3 - @k2_lib.K2	72A7 72C6
IMVP6_BOOT3_RC	IMVP6_BOOT3_RC - @k2_lib.K2	72A7 72C5
IMVP6_COMP	IMVP6_COMP - @k2_lib.K2	71A8 71B7
IMVP6_COMP_RC	IMVP6_COMP_RC - @k2_lib.K2	71B8
IMVP6_DFB	IMVP6_DFB - @k2_lib.K2	71A8 71B5
IMVP6_DROOP	IMVP6_DROOP - @k2_lib.K2	71A8 71B4
IMVP6_FB	IMVP6_FB - @k2_lib.K2	71A8 71B7
IMVP6_FCCM	IMVP6_FCCM - @k2_lib.K2	71A8 71C5 72C7
IMVP6_FET_RC1	IMVP6_FET_RC1 - @k2_lib.K2	71A6 71C3
IMVP6_FET_RC2	IMVP6_FET_RC2 - @k2_lib.K2	71A4 71B3
IMVP6_FET_RC3	IMVP6_FET_RC3 - @k2_lib.K2	72A7 72C3
IMVP6_ISEN1	IMVP6_ISEN1 - @k2_lib.K2	71A6 71C3 72C1
IMVP6_ISEN2	IMVP6_ISEN2 - @k2_lib.K2	71A4 71C5
IMVP6_ISEN3	IMVP6_ISEN3 - @k2_lib.K2	71C5 72A7 72B1
IMVP6_LGATE1	IMVP6_LGATE1 - @k2_lib.K2	71A6 71D4
IMVP6_LGATE2	IMVP6_LGATE2 - @k2_lib.K2	71A4 71C4
IMVP6_LGATE3	IMVP6_LGATE3 - @k2_lib.K2	72A7 72C6
IMVP6_NTC	IMVP6_NTC - @k2_lib.K2	71C7
IMVP6_NTC_R	IMVP6_NTC_R - @k2_lib.K2	71C8
IMVP6_OCSET	IMVP6_OCSET - @k2_lib.K2	71A8 71B5
IMVP6_PHASE1	IMVP6_PHASE1 - @k2_lib.K2	71A6 71D4 108D1
IMVP6_PHASE2	IMVP6_PHASE2 - @k2_lib.K2	71A4 71C4 108D1
IMVP6_PHASE3	IMVP6_PHASE3 - @k2_lib.K2	72A7 72C6 108D1
IMVP6_PMON	IMVP6_PMON - @k2_lib.K2	53C8 71C5

8 7 6 5 4 3 2 1

IMVP6_PWM1	IMVP6_PWM1 - @k2_lib.K2	71A6 71D5
IMVP6_PWM2	IMVP6_PWM2 - @k2_lib.K2	71A4 71C5
IMVP6_PWM3	IMVP6_PWM3 - @k2_lib.K2	71C5 72A7 72C7
IMVP6_RBIAS	IMVP6_RBIAS - @k2_lib.K2	71A8 71B7
IMVP6_SOFT	IMVP6_SOFT - @k2_lib.K2	71A8 71C7
IMVP6_UGATE1	IMVP6_UGATE1 - @k2_lib.K2	71A6 71D4
IMVP6_UGATE2	IMVP6_UGATE2 - @k2_lib.K2	71A4 71C4
IMVP6_UGATE3	IMVP6_UGATE3 - @k2_lib.K2	72A7 72C6
IMVP6_VDIFF	IMVP6_VDIFF - @k2_lib.K2	71A8 71B7
IMVP6_VDIFF_RC	IMVP6_VDIFF_RC - @k2_lib.K2	71B8
IMVP6_VID<0>	IMVP6_VID<0> - @k2_lib.K2	12C1 71C7
IMVP6_VID<6..0>	IMVP6_VID<6..0> - @k2_lib.K2	100A3
IMVP6_VID<1>	IMVP6_VID<1> - @k2_lib.K2	12C1 71C7
IMVP6_VID<2>	IMVP6_VID<2> - @k2_lib.K2	12C1 71C7
IMVP6_VID<3>	IMVP6_VID<3> - @k2_lib.K2	12C1 71C7
IMVP6_VID<4>	IMVP6_VID<4> - @k2_lib.K2	12C1 71C7
IMVP6_VID<5>	IMVP6_VID<5> - @k2_lib.K2	12C1 71C7
IMVP6_VID<6>	IMVP6_VID<6> - @k2_lib.K2	12C1 71C7
IMVP6_VO	IMVP6_VO - @k2_lib.K2	71A8 71B4 72C1
IMVP6_VO1	IMVP6_VO1 - @k2_lib.K2	71A6 71D1 72A7
IMVP6_VO2	IMVP6_VO2 - @k2_lib.K2	71A4 71B1 72A7
IMVP6_VO3	IMVP6_VO3 - @k2_lib.K2	72A7 72A7 72C2
IMVP6_VO_R	IMVP6_VO_R - @k2_lib.K2	71B4
IMVP6_VR_TT_L	IMVP6_VR_TT_L - @k2_lib.K2	71C7
IMVP6_VSEN_N	IMVP6_VSEN_N - @k2_lib.K2	71A5 100A3
IMVP6_VSEN_P	IMVP6_VSEN_P - @k2_lib.K2	71A5 100A3
IMVP6_VSUM	IMVP6_VSUM - @k2_lib.K2	71A8 71C4 72B1
IMVP6_VSUM1	IMVP6_VSUM1 - @k2_lib.K2	71A6 71C2 72A7
IMVP6_VSUM2	IMVP6_VSUM2 - @k2_lib.K2	71A4 71B2 72A7
IMVP6_VSUM3	IMVP6_VSUM3 - @k2_lib.K2	72A7 72A7 72C3
IMVP6_VW	IMVP6_VW - @k2_lib.K2	71A8 71B7
IMVP_DPRSLPVR	IMVP_DPRSLPVR - @k2_lib.K2	71C7 100B3
IMVP_PGD_IN	IMVP_PGD_IN - @k2_lib.K2	70B3
IMVP_VR_ON	IMVP_VR_ON - @k2_lib.K2	7C4 49C8 71C7
INT_PIRQA_L	INT_PIRQA_L - @k2_lib.K2	24A4 24A8 104C3
INT_PIRQB_L	INT_PIRQB_L - @k2_lib.K2	24A4 24A8 104C3
INT_PIRQC_L	INT_PIRQC_L - @k2_lib.K2	24A4 24A8 104C3
INT_PIRQD_L	INT_PIRQD_L - @k2_lib.K2	24A4 24A8 104C3
INT_PIRQE_L	INT_PIRQE_L - @k2_lib.K2	24A4 24A6 98B7 104C3
INT_PIRQF_L	INT_PIRQF_L - @k2_lib.K2	24A4 24A6 104C3
INT_SERIRQ	INT_SERIRQ - @k2_lib.K2	7D4 25C8 49C8 51B4
INV_EN_BL_OR_PANEL_ID	INV_EN_BL_OR_PANEL_ID - @k2_lib.K2	6D6 28B2 85A3
IPHS_SW_INT_TO_SB	IPHS_SW_INT_TO_SB - @k2_lib.K2	98C6
IPHS_SW_SUPBIAS_EN_L	IPHS_SW_SUPBIAS_EN_L - @k2_lib.K2	98C6
ISENSE_CAL_EN	ISENSE_CAL_EN - @k2_lib.K2	49B8 50A2 53A8
ISENSE_CAL_EN_L	ISENSE_CAL_EN_L - @k2_lib.K2	53B8
ISENSE_CAL_EN_LS12V	ISENSE_CAL_EN_LS12V - @k2_lib.K2	53B7
ISENSE_CAL_EN_L_R	ISENSE_CAL_EN_L_R - @k2_lib.K2	53B8
ITP_CPURST_L	ITP_CPURST_L - @k2_lib.K2	100A3
ITS_ALIVE	ITS_ALIVE - @k2_lib.K2	6A7
ITS_PLUGGED_IN	ITS_PLUGGED_IN - @k2_lib.K2	6A8
LAN_ENERGY_DET	LAN_ENERGY_DET - @k2_lib.K2	23C6 28A2
	TP_LAN_ENERGY_DET - @k2_lib.K2	28A1
LAN_PHYPC	LAN_PHYPC - @k2_lib.K2	25A5 25C5
LCD_PWM	LCD_PWM - @k2_lib.K2	6D8 90B1
LCD_PWREN_DIV	LCD_PWREN_DIV - @k2_lib.K2	90C8
LCD_PWREN_L	LCD_PWREN_L - @k2_lib.K2	90B7
LCD_PWREN_L_RC	LCD_PWREN_L_RC - @k2_lib.K2	90C7
LCD_SHOULD_ON	LCD_SHOULD_ON - @k2_lib.K2	6A6
LED4300_1	LED4300_1 - @k2_lib.K2	39A7
LED4301_1	LED4301_1 - @k2_lib.K2	39A7
LED4302_1	LED4302_1 - @k2_lib.K2	39A6
LED4303_1	LED4303_1 - @k2_lib.K2	39A6
LINDACARD_GPIO	LINDACARD_GPIO - @k2_lib.K2	7C4 25A7 25D5 51B4
LPC_AD<0>	LPC_AD<0> - @k2_lib.K2	7D4 23D4 49C8 51C6
LPC_AD<1>	LPC_AD<1> - @k2_lib.K2	7A8 7C6 7D4 23D4 49C8 51C6
LPC_AD<2>	LPC_AD<2> - @k2_lib.K2	7D4 23D4 49C8 51C4
LPC_AD<3>	LPC_AD<3> - @k2_lib.K2	7D4 23D4 49C8 51C4
LPC_FRAME_L	LPC_FRAME_L - @k2_lib.K2	7D4 23D4 49C8 51B6
LVDS_A_CLK_N	LVDS_A_CLK_N - @k2_lib.K2	15C5 22D8
	TP_LVDS_A_CLK_N - @k2_lib.K2	22D7
LVDS_A_CLK_P	LVDS_A_CLK_P - @k2_lib.K2	15C5 22D8
	TP_LVDS_A_CLK_P - @k2_lib.K2	22D7
LVDS_A_DATA_N<0>	LVDS_A_DATA_N<0> - @k2_lib.K2	15C5 22D8
LVDS_A_DATA_N<1>	LVDS_A_DATA_N<1> - @k2_lib.K2	15C5 22C8
LVDS_A_DATA_N<2>	LVDS_A_DATA_N<2> - @k2_lib.K2	15C5 22C8
LVDS_A_DATA_P<0>	LVDS_A_DATA_P<0> - @k2_lib.K2	15C5 22C8
LVDS_A_DATA_P<1>	LVDS_A_DATA_P<1> - @k2_lib.K2	15C5 22C8
LVDS_A_DATA_P<2>	LVDS_A_DATA_P<2> - @k2_lib.K2	15C5 22C8
LVDS_BKLT_CTL	LVDS_BKLT_CTL - @k2_lib.K2	15D5 22D8
	TP_LVDS_BKLT_CTL - @k2_lib.K2	22D7
LVDS_BKLT_EN	LVDS_BKLT_EN - @k2_lib.K2	15D5 22D8
	TP_LVDS_BKLT_EN - @k2_lib.K2	7B3 22D7
LVDS_B_CLK_N	LVDS_B_CLK_N - @k2_lib.K2	15C5 22D8
	TP_LVDS_B_CLK_N - @k2_lib.K2	22D7
LVDS_B_CLK_P	LVDS_B_CLK_P - @k2_lib.K2	15C5 22D8
	TP_LVDS_B_CLK_P - @k2_lib.K2	22D7
LVDS_B_DATA_N<0>	LVDS_B_DATA_N<0> - @k2_lib.K2	15C5 22C8
LVDS_B_DATA_N<1>	LVDS_B_DATA_N<1> - @k2_lib.K2	15C5 22C8
LVDS_B_DATA_N<2>	LVDS_B_DATA_N<2> - @k2_lib.K2	15C5 22C8
LVDS_B_DATA_P<0>	LVDS_B_DATA_P<0> - @k2_lib.K2	15C5 22C8
LVDS_B_DATA_P<1>	LVDS_B_DATA_P<1> - @k2_lib.K2	15C5 22C8
LVDS_B_DATA_P<2>	LVDS_B_DATA_P<2> - @k2_lib.K2	15C5 22C8
LVDS_IBG	LVDS_IBG - @k2_lib.K2	15D5 22D8
	TP_LVDS_IBG - @k2_lib.K2	22D7
LVDS_L_CLK_N	LVDS_L_CLK_N - @k2_lib.K2	85B4 90A6 108C3
LVDS_L_CLK_P	LVDS_L_CLK_P - @k2_lib.K2	85B4 90A8 108C3
LVDS_L_DATA_N<0>	LVDS_L_DATA_N<0> - @k2_lib.K2	85A4 90A6
LVDS_L_DATA_N<3..0>	LVDS_L_DATA_N<3..0> - @k2_lib.K2	108C3
LVDS_L_DATA_N<1>	LVDS_L_DATA_N<1> - @k2_lib.K2	85B4 90A8
LVDS_L_DATA_N<2>	LVDS_L_DATA_N<2> - @k2_lib.K2	85B4 90A6
LVDS_L_DATA_N<3>	LVDS_L_DATA_N<3> - @k2_lib.K2	85B4 90A6
LVDS_L_DATA_P<0>	LVDS_L_DATA_P<0> - @k2_lib.K2	85A4 90A8
LVDS_L_DATA_P<3..0>	LVDS_L_DATA_P<3..0> - @k2_lib.K2	108C3
LVDS_L_DATA_P<1>	LVDS_L_DATA_P<1> - @k2_lib.K2	85B4 90A6
LVDS_L_DATA_P<2>	LVDS_L_DATA_P<2> - @k2_lib.K2	85B4 90A8
LVDS_L_DATA_P<3>	LVDS_L_DATA_P<3> - @k2_lib.K2	85B4 90A8
LVDS_U_CLK_N	LVDS_U_CLK_N - @k2_lib.K2	85B4 90A6 108C3
LVDS_U_CLK_P	LVDS_U_CLK_P - @k2_lib.K2	85B4 90A8 108C3
LVDS_U_DATA_N<0>	LVDS_U_DATA_N<0> - @k2_lib.K2	85B4 90A8
LVDS_U_DATA_N<3..0>	LVDS_U_DATA_N<3..0> - @k2_lib.K2	108C3
LVDS_U_DATA_N<1>	LVDS_U_DATA_N<1> - @k2_lib.K2	85B4 90A8
LVDS_U_DATA_N<2>	LVDS_U_DATA_N<2> - @k2_lib.K2	85B4 90A8
LVDS_U_DATA_N<3>	LVDS_U_DATA_N<3> - @k2_lib.K2	85B4 90A6
LVDS_U_DATA_P<0>	LVDS_U_DATA_P<0> - @k2_lib.K2	85B4 90A6
LVDS_U_DATA_P<3..0>	LVDS_U_DATA_P<3..0> - @k2_lib.K2	108C3
LVDS_U_DATA_P<1>	LVDS_U_DATA_P<1> - @k2_lib.K2	85B4 90A6
LVDS_U_DATA_P<2>	LVDS_U_DATA_P<2> - @k2_lib.K2	85B4 90A6
LVDS_U_DATA_P<3>	LVDS_U_DATA_P<3> - @k2_lib.K2	85B4 90A8
LVDS_VDD_EN	LVDS_VDD_EN - @k2_lib.K2	15D5 22D8
	TP_LVDS_VDD_EN - @k2_lib.K2	22D7
LVDS_VREFH	LVDS_VREFH - @k2_lib.K2	15D5 22D8
	TP_LVDS_VREFH - @k2_lib.K2	22D7
LVDS_VREFL	LVDS_VREFL - @k2_lib.K2	15D5 22D8
	TP_LVDS_VREFL - @k2_lib.K2	22D7
MCH_CORES0_BOOT	MCH_CORES0_BOOT - @k2_lib.K2	74C4
MCH_CORES0_BOOT_R	MCH_CORES0_BOOT_R - @k2_lib.K2	74C3
MCH_CORES0_ISEN	MCH_CORES0_ISEN - @k2_lib.K2	74C4
MCH_CORES0_LGATE	MCH_CORES0_LGATE - @k2_lib.K2	74C3
MCH_CORES0_OCSET	MCH_CORES0_OCSET - @k2_lib.K2	74B4
MCH_CORES0_SNUBBER_R	MCH_CORES0_SNUBBER_R - @k2_lib.K2	74C2
MCH_CORES0_SOFT	MCH_CORES0_SOFT - @k2_lib.K2	74C4
MCH_CORES0_SWITCHNODE	MCH_CORES0_SWITCHNODE - @k2_lib.K2	74C3 108D1
MCH_CORES0_UGATE	MCH_CORES0_UGATE - @k2_lib.K2	74C4
MCH_CORES0_VSEN	MCH_CORES0_VSEN - @k2_lib.K2	74B3
MEMVTT_VREF	MEMVTT_VREF - @k2_lib.K2	75A4
MEM_A_A<0>	MEM_A_A<0> - @k2_lib.K2	17C5 31B3 33C6
MEM_A_A<14..0>	MEM_A_A<14..0> - @k2_lib.K2	102D3
MEM_A_A<1>	MEM_A_A<1> - @k2_lib.K2	17C5 31B6 33C6
MEM_A_A<2>	MEM_A_A<2> - @k2_lib.K2	17B5 31B3 33C6
MEM_A_A<3>	MEM_A_A<3> - @k2_lib.K2	17B5 31B6 33C6
MEM_A_A<4>	MEM_A_A<4> - @k2_lib.K2	17B5 31C3 33C6
MEM_A_A<5>	MEM_A_A<5> - @k2_lib.K2	17B5 31C6 33C6
MEM_A_A<6>	MEM_A_A<6> - @k2_lib.K2	17B5 31C3 33C6
MEM_A_A<7>	MEM_A_A<7> - @k2_lib.K2	17B5 31C3 33C6
MEM_A_A<8>	MEM_A_A<8> - @k2_lib.K2	17B5 31C6 33C6
MEM_A_A<9>	MEM_A_A<9> - @k2_lib.K2	17B5 31C6 33C6
MEM_A_A<10>	MEM_A_A<10> - @k2_lib.K2	17B5 31B6 33C6
MEM_A_A<11>	MEM_A_A<11> - @k2_lib.K2	17B5 31C3 33C6
MEM_A_A<12>	MEM_A_A<12> - @k2_lib.K2	17B5 31C6 33C6
MEM_A_A<13>	MEM_A_A<13> - @k2_lib.K2	17B5 31B3 33C6
MEM_A_A<14>	MEM_A_A<14> - @k2_lib.K2	16C6 31C3 33C6
MEM_A_BS<0>	MEM_A_BS<0> - @k2_lib.K2	17D5 31B6 33B6
MEM_A_BS<2..0>	MEM_A_BS<2..0> - @k2_lib.K2	102D3
MEM_A_BS<1>	MEM_A_BS<1> - @k2_lib.K2	17D5 31B3 33B6
MEM_A_BS<2>	MEM_A_BS<2> - @k2_lib.K2	17D5 31C6 33B6
MEM_A_CAS_L	MEM_A_CAS_L - @k2_lib.K2	17D5 31B6 33B6 102D3
MEM_A_DM<0>	MEM_A_DM<0> - @k2_lib.K2	17D5 31D3 102C3
MEM_A_DM<1>	MEM_A_DM<1> - @k2_lib.K2	17D5 31D3 102C3
MEM_A_DM<2>	MEM_A_DM<2> - @k2_lib.K2	17C5 31C3 102C3
MEM_A_DM<3>	MEM_A_DM<3> - @k2_lib.K2	17C5 31C6 102C3
MEM_A_DM<4>	MEM_A_DM<4> - @k2_lib.K2	17C5 31B3 102C3
MEM_A_DM<5>	MEM_A_DM<5> - @k2_lib.K2	17C5 31B6 102C3
MEM_A_DM<6>	MEM_A_DM<6> - @k2_lib.K2	17C5 31A3 102C3
MEM_A_DM<7>	MEM_A_DM<7> - @k2_lib.K2	17C5 31A6 102C3
MEM_A_DQ<0>	MEM_A_DQ<0> - @k2_lib.K2	17D8 31D6
MEM_A_DQ<6..0>	MEM_A_DQ<6..0> - @k2_lib.K2	102D3
MEM_A_DQ<1>	MEM_A_DQ<1> - @k2_lib.K2	17D8 31D6
MEM_A_DQ<2>	MEM_A_DQ<2> - @k2_lib.K2	17D8 31D6
MEM_A_DQ<3>	MEM_A_DQ<3> - @k2_lib.K2	17D8 31D6
MEM_A_DQ<4>	MEM_A_DQ<4> - @k2_lib.K2	17D8 31D3
MEM_A_DQ<5>	MEM_A_DQ<5> - @k2_lib.K2	17D8 31D3
MEM_A_DQ<6>	MEM_A_DQ<6> - @k2_lib.K2	17D8 31D3
MEM_A_DQ<7>	MEM_A_DQ<7> - @k2_lib.K2	7C7 17D8 31D3 102D3
MEM_A_DQ<8>	MEM_A_DQ<8> - @k2_lib.K2	17C8 31D6
MEM_A_DQ<13..8>	MEM_A_DQ<13..8> - @k2_lib.K2	102D3
MEM_A_DQ<9>	MEM_A_DQ<9> - @k2_lib.K2	17C8 31D6
MEM_A_DQ<10>	MEM_A_DQ<10> - @k2_lib.K2	17C8 31D6
MEM_A_DQ<11>	MEM_A_DQ<11> - @k2_lib.K2	17C8 31D6
MEM_A_DQ<12>	MEM_A_DQ<12> - @k2_lib.K2	17C8 31D3
MEM_A_DQ<13>	MEM_A_DQ<13> - @k2_lib.K2	17C8 31D3
MEM_A_DQ<14>	MEM_A_DQ<14> - @k2_lib.K2	7C7 17C8 31D3 102D3
MEM_A_DQ<15>	MEM_A_DQ<15> - @k2_lib.K2	17C8 31D3 102C3
MEM_A_DQ<16>	MEM_A_DQ<16> - @k2_lib.K2	7B7 17C8 31D6 102C3
MEM_A_DQ<17>	MEM_A_DQ<17> - @k2_lib.K2	17C8 31D6
MEM_A_DQ<23..17>	MEM_A_DQ<23..17> - @k2_lib.K2	102C3
MEM_A_DQ<18>	MEM_A_DQ<18> - @k2_lib.K2	17C8 31C6
MEM_A_DQ<19>	MEM_A_DQ<19> - @k2_lib.K2	17C8 31C6
MEM_A_DQ<20>	MEM_A_DQ<20> - @k2_lib.K2	17C8 31D3
MEM_A_DQ<21>	MEM_A_DQ<21> - @k2_lib.K2	17C8 31D3
MEM_A_DQ<22>	MEM_A_DQ<22> - @k2_lib.K2	17C8 31C3
MEM_A_DQ<23>	MEM_A_DQ<23> - @k2_lib.K2	17C8 31C3
MEM_A_DQ<24>	MEM_A_DQ<24> - @k2_lib.K2	17C8 31C6 102C3
MEM_A_DQ<25>	MEM_A_DQ<25> - @k2_lib.K2	7B7 17C8 31C6 102C3
MEM_A_DQ<26>	MEM_A_DQ<26> - @k2_lib.K2	17C8 31C6
MEM_A_DQ<31..26>	MEM_A_DQ<31..26> - @k2_lib.K2	102C3
MEM_A_DQ<27>	MEM_A_DQ<27> - @k2_lib.K2	17C8 31C6
MEM_A_DQ<28>	MEM_A_DQ<28> - @k2_lib.K2	17C8 31C3
MEM_A_DQ<29>	MEM_A_DQ<29> - @k2_lib.K2	17C8 31C3
MEM_A_DQ<30>	MEM_A_DQ<30> - @k2_lib.K2	17C8 31C3
MEM_A_DQ<31>	MEM_A_DQ<31> - @k2_lib.K2	17C8 31C3
MEM_A_DQ<32>	MEM_A_DQ<32> - @k2_lib.K2	17C8 31B6
MEM_A_DQ<38..32>	MEM_A_DQ<38..32> - @k2_lib.K2	102C3
MEM_A_DQ<33>	MEM_A_DQ<33> - @k2_lib.K2	17C8 31B6
MEM_A_DQ<34>	MEM_A_DQ<34> - @k2_lib.K2	17B8 31B6
MEM_A_DQ<35>	MEM_A_DQ<35> - @k2_lib.K2	17B8 31B6
MEM_A_DQ<36>	MEM_A_DQ<36> - @k2_lib.K2	17B8 31B3
MEM_A_DQ<37>	MEM_A_DQ<37> - @k2_lib.K2	17B8 31B3
MEM_A_DQ<38>	MEM_A_DQ<38> - @k2_lib.K2	17B8 31B3
MEM_A_DQ<39>	MEM_A_DQ<39> - @k2_lib.K2	7B7 17B8 31B3 102C3
MEM_A_DQ<40>	MEM_A_DQ<40> - @k2_lib.K2	17B8 31B6
MEM_A_DQ<46..40>	MEM_A_DQ<46..40> - @k2_lib.K2	102C3
MEM_A_DQ<41>	MEM_A_DQ<41> - @k2_lib.K2	17B8 31B6
MEM_A_DQ<42>	MEM_A_DQ<42> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<43>	MEM_A_DQ<43> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<44>	MEM_A_DQ<44> - @k2_lib.K2	17B8 31B3
MEM_A_DQ<45>	MEM_A_DQ<45> - @k2_lib.K2	17B8 31B3
MEM_A_DQ<46>	MEM_A_DQ<46> - @k2_lib.K2	17B8 31A3
MEM_A_DQ<47>	MEM_A_DQ<47> - @k2_lib.K2	7B7 17B8 31A3 102C3
MEM_A_DQ<48>	MEM_A_DQ<48> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<53..48>	MEM_A_DQ<53..48> - @k2_lib.K2	102C3
MEM_A_DQ<49>	MEM_A_DQ<49> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<50>	MEM_A_DQ<50> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<51>	MEM_A_DQ<51> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<52>	MEM_A_DQ<52> - @k2_lib.K2	17B8 31A3
MEM_A_DQ<53>	MEM_A_DQ<53> - @k2_lib.K2	17B8 31A3
MEM_A_DQ<54>	MEM_A_DQ<54> - @k2_lib.K2	7B7 17B8 31A3 102C3
MEM_A_DQ<55>	MEM_A_DQ<55> - @k2_lib.K2	17B8 31A3 102C3
MEM_A_DQ<56>	MEM_A_DQ<56> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<58..56>	MEM_A_DQ<58..56> - @k2_lib.K2	102C3
MEM_A_DQ<57>	MEM_A_DQ<57> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<58>	MEM_A_DQ<58> - @k2_lib.K2	17B8 31A6
MEM_A_DQ<59>	MEM_A_DQ<59> - @k2_lib.K2	7B7 17B8 31A6 102C3
MEM_A_DQ<60>	MEM_A_DQ<60> - @k2_lib.K2	17A8 31A3
MEM_A_DQ<63..60>	MEM_A_DQ<63..60> - @k2_lib.K2	102C3
MEM_A_DQ<61>	MEM_A_DQ<61> - @k2_lib.K2	17A8 31A3
MEM_A_DQ<62>	MEM_A_DQ<62> - @k2_lib.K2	17A8 31A3
MEM_A_DQ<63>	MEM_A_DQ<63> - @k2_lib.K2	17A8 31A3
MEM_A_DQS_N<0>	MEM_A_DQS_N<0> - @k2_lib.K2	7B7 17C5 31D6 102B3
MEM_A_DQS_N<1>	MEM_A_DQS_N<1> - @k2_lib.K2	7B7 17C5 31D6 102B3
MEM_A_DQS_N<2>	MEM_A_DQS_N<2> - @k2_lib.K2	7B7 17C5 31C6 102B3
MEM_A_DQS_N<3>	MEM_A_DQS_N<3> - @k2_lib.K2	7B7 17C5 31C3 102B3
MEM_A_DQS_N<4>	MEM_A_DQS_N<4> - @k2_lib.K2	7B7 17C5 31B6 102B3
MEM_A_DQS_N<5>	MEM_A_DQS_N<5> - @k2_lib.K2	7B7 17C5 31B3 102B3
MEM_A_DQS_N<6>	MEM_A_DQS_N<6> - @k2_lib.K2	7B7 17C5 31A6 102B3
MEM_A_DQS_N<7>	MEM_A_DQS_N<7> - @k2_lib.K2	7B7 17C5 31A3 102B3
MEM_A_DQS_P<0>	MEM_A_DQS_P<0> - @k2_lib.K2	7B7 17C5 31D6 102B3
MEM_A_DQS_P<1>	MEM_A_DQS_P<1> - @k2_lib.K2	7B7 17C5 31D6 102B3
MEM_A_DQS_P<2>	MEM_A_DQS_P<2> - @k2_lib.K2	7B7 17C5 31C6 102B3
MEM_A_DQS_P<3>	MEM_A_DQS_P<3> - @k2_lib.K2	7B7 17C5 31C3 102B3
MEM_A_DQS_P<4>	MEM_A_DQS_P<4> - @k2_lib.K2	7B7 17C5 31B6 102B3
MEM_A_DQS_P<5>	MEM_A_DQS_P<5> - @k2_lib.K2	7B7 17C5 31B3 102B3
MEM_A_DQS_P<6>	MEM_A_DQS_P<6> - @k2_lib.K2	7B7 17C5 31A6 102B3
MEM_A_DQS_P<7>	MEM_A_DQS_P<7> - @k2_lib.K2	7B7 17C5 31A3 102B3
MEM_A_RAS_L	MEM_A_RAS_L - @k2_lib.K2	17B5 31B3 33B6 102D3
MEM_A_SA<0>	MEM_A_SA<0> - @k2_lib.K2	31A4
MEM_A_SA<1>	MEM_A_SA<1> - @k2_lib.K2	31A4
MEM_A_WE_L	MEM_A_WE_L - @k2_lib.K2	17B5 31B6 33B6 102D3
MEM_B_A<0>	MEM_B_A<0> - @k2_lib.K2	17C1 32B3 33B6
MEM_B_A<14..0>	MEM_B_A<14..0> - @k2_lib.K2	102D1
MEM_B_A<1>	MEM_B_A<1> - @k2_lib.K2	17C1 32B6 33B6
MEM_B_A<2>	MEM_B_A<2> - @k2_lib.K2	17B1 32B3 33B6
MEM_B_A<3>	MEM_B_A<3> - @k2_lib.K2	17B1 32B6 33B6
MEM_B_A<4>	MEM_B_A<4> - @k2_lib.K2	17B1 32C3 33B6
MEM_B_A<5>	MEM_B_A<5> - @k2_lib.K2	17B1 32C6 33B6
MEM_B_A<6>	MEM_B_A<6> - @k2_lib.K2	17B1 32C3 33B6
MEM_B_A<7>	MEM_B_A<7> - @k2_lib.K2	17B1 32C3 33B6
MEM_B_A<8>	MEM_B_A<8> - @k2_lib.K2	17B1 32C6 33B6
MEM_B_A<9>	MEM_B_A<9> - @k2_lib.K2	17B1 32C6 33B6
MEM_B_A<10>	MEM_B_A<10> - @k2_lib.K2	17B1 32B6 33B6
MEM_B_A<11>	MEM_B_A<11> - @k2_lib.K2	17B1 32C3 33A6
MEM_B_A<12>	MEM_B_A<12> - @k2_lib.K2	17B1 32C6 33A6
MEM_B_A<13>	MEM_B_A<13> - @k2_lib.K2	17B1 32B3 33A6
MEM_B_A<14>	MEM_B_A<14> - @k2_lib.K2	16C6 32C3 33A6
MEM_B_BS<0>	MEM_B_BS<0> - @k2_lib.K2	17D1 32B6 33A6
MEM_B_BS<2..0>	MEM_B_BS<2..0> - @k2_lib.K2	102D1
MEM_B_BS<1>	MEM_B_BS<1> - @k2_lib.K2	17D1 32B3 33A6
MEM_B_BS<2>	MEM_B_BS<2> - @k2_lib.K2	17D1 32C6 33A6
MEM_B_CAS_L	MEM_B_CAS_L - @k2_lib.K2	17D1 32B6 33A6 102D1
MEM_B_DM<0>	MEM_B_DM<0> - @k2_lib.K2	17D1 32D3 102C1
MEM_B_DM<1>	MEM_B_DM<1> - @k2_lib.K2	17D1 32D3 102C1
MEM_B_DM<2>	MEM_B_DM<2> - @k2_lib.K2	17C1 32C3 102C1
MEM_B_DM<3>	MEM_B_DM<3> - @k2_lib.K2	17C1 32C6 102C1
MEM_B_DM<4>	MEM_B_DM<4> - @k2_lib.K2	17C1 32B3 102C1
MEM_B_DM<5>	MEM_B_DM<5> - @k2_lib.K2	17C1 32B6 102C1
MEM_B_DM<6>	MEM_B_DM<6> - @k2_lib.K2	17C1 32A3 102C1
MEM_B_DM<7>	MEM_B_DM<7> - @k2_lib.K2	17C1 32A6 102C1
MEM_B_DQ<0>	MEM_B_DQ<0> - @k2_lib.K2	17D4 32D6
MEM_B_DQ<5..0>	MEM_B_DQ<5..0> - @k2_lib.K2	102D1
MEM_B_DQ<1>	MEM_B_DQ<1> - @k2_lib.K2	17D4 32D6
MEM_B_DQ<2>	MEM_B_DQ<2> - @k2_lib.K2	17D4 32D6
MEM_B_DQ<3>	MEM_B_DQ<3> - @k2_lib.K2	17D4 32D6
MEM_B_DQ<4>	MEM_B_DQ<4> - @k2_lib.K2	17D4 32D3
MEM_B_DQ<5>	MEM_B_DQ<5> - @k2_lib.K2	17D4 32D3
MEM_B_DQ<6>	MEM_B_DQ<6> - @k2_lib.K2	7B7 17D4 32D3 102D1
MEM_B_DQ<7>	MEM_B_DQ<7> - @k2_lib.K2	17D4 32D3 102D1
MEM_B_DQ<8>	MEM_B_DQ<8> - @k2_lib.K2	7B7 17C4 32D6 102D1
MEM_B_DQ<9>	MEM_B_DQ<9> - @k2_lib.K2	17C4 32D6
MEM_B_DQ<15..9>	MEM_B_DQ<15..9> - @k2_lib.K2	102D1
MEM_B_DQ<10>	MEM_B_DQ<10> - @k2_lib.K2	17C4 32D6
MEM_B_DQ<11>	MEM_B_DQ<11> - @k2_lib.K2	17C4 32D6
MEM_B_DQ<12>	MEM_B_DQ<12> - @k2_lib.K2	17C4 32D3
MEM_B_DQ<13>	MEM_B_DQ<13> - @k2_lib.K2	17C4 32D3
MEM_B_DQ<14>	MEM_B_DQ<14> - @k2_lib.K2	17C4 32D3
MEM_B_DQ<15>	MEM_B_DQ<15> - @k2_lib.K2	17C4 32D3
MEM_B_DQ<16>	MEM_B_DQ<16> - @k2_lib.K2	17C4 32D6
MEM_B_DQ<22..16>	MEM_B_DQ<22..16> - @k2_lib.K2	102D1
MEM_B_DQ<17>	MEM_B_DQ<17> - @k2_lib.K2	17C4 32D6
MEM_B_DQ<18>	MEM_B_DQ<18> - @k2_lib.K2	17C4 32C6
MEM_B_DQ<19>	MEM_B_DQ<19> - @k2_lib.K2	17C4 32C6
MEM_B_DQ<20>	MEM_B_DQ<20> - @k2_lib.K2	17C4 32D3
MEM_B_DQ<21>	MEM_B_DQ<21> - @k2_lib.K2	17C4 32D3
MEM_B_DQ<22>	MEM_B_DQ<22> - @k2_lib.K2	17C4 32C3
MEM_B_DQ<23>	MEM_B_DQ<23> - @k2_lib.K2	7B7 17C4 32C3 102D1
MEM_B_DQ<24>	MEM_B_DQ<24> - @k2_lib.K2	17C4 32C6 102C1
MEM_B_DQ<25>	MEM_B_DQ<25> - @k2_lib.K2	7B7 17C4 32C6 102C1
MEM_B_DQ<26>	MEM_B_DQ<26> - @k2_lib.K2	17C4 32C6
MEM_B_DQ<31..26>	MEM_B_DQ<31..26> - @k2_lib.K2	102C1
MEM_B_DQ<27>	MEM_B_DQ<27> - @k2_lib.K2	17C4 32C6
MEM_B_DQ<28>	MEM_B_DQ<28> - @k2_lib.K2	17C4 32C3
MEM_B_DQ<29>	MEM_B_DQ<29> - @k2_lib.K2	17C4 32C3
MEM_B_DQ<30>	MEM_B_DQ<30> - @k2_lib.K2	17C4 32C3
MEM_B_DQ<31>	MEM_B_DQ<31> - @k2_lib.K2	17C4 32C3
MEM_B_DQ<32>	MEM_B_DQ<32> - @k2_lib.K2	17C4 32B6
MEM_B_DQ<37..32>	MEM_B_DQ<37..32> - @k2_lib.K2	102C1
MEM_B_DQ<33>	MEM_B_DQ<33> - @k2_lib.K2	17C4 32B6
MEM_B_DQ<34>	MEM_B_DQ<34> - @k2_lib.K2	17B4 32B6
MEM_B_DQ<35>	MEM_B_DQ<35> - @k2_lib.K2	17B4 32B6
MEM_B_DQ<36>	MEM_B_DQ<36> - @k2_lib.K2	17B4 32B3
MEM_B_DQ<37>	MEM_B_DQ<37> - @k2_lib.K2	17B4 32B3
MEM_B_DQ<38>	MEM_B_DQ<38> - @k2_lib.K2	7A7 17B4 32B3 102C1
MEM_B_DQ<39>	MEM_B_DQ<39> - @k2_lib.K2	17B4 32B3 102C1
MEM_B_DQ<40>	MEM_B_DQ<40> - @k2_lib.K2	17B4 32B6
MEM_B_DQ<43..40>	MEM_B_DQ<43..40> - @k2_lib.K2	102C1
MEM_B_DQ<41>	MEM_B_DQ<41> - @k2_lib.K2	17B4 32B6
MEM_B_DQ<42>	MEM_B_DQ<42> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<43>	MEM_B_DQ<43> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<44>	MEM_B_DQ<44> - @k2_lib.K2	7A7 17B4 32B3 102C1
MEM_B_DQ<45>	MEM_B_DQ<45> - @k2_lib.K2	17B4 32B3
MEM_B_DQ<47..45>	MEM_B_DQ<47..45> - @k2_lib.K2	102C1
MEM_B_DQ<46>	MEM_B_DQ<46> - @k2_lib.K2	17B4 32A3
MEM_B_DQ<47>	MEM_B_DQ<47> - @k2_lib.K2	17B4 32A3
MEM_B_DQ<48>	MEM_B_DQ<48> - @k2_lib.K2	7A7 17B4 32A6 102C1
MEM_B_DQ<49>	MEM_B_DQ<49> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<55..49>	MEM_B_DQ<55..49> - @k2_lib.K2	102C1
MEM_B_DQ<50>	MEM_B_DQ<50> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<51>	MEM_B_DQ<51> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<52>	MEM_B_DQ<52> - @k2_lib.K2	17B4 32A3
MEM_B_DQ<53>	MEM_B_DQ<53> - @k2_lib.K2	17B4 32A3
MEM_B_DQ<54>	MEM_B_DQ<54> - @k2_lib.K2	17B4 32A3
MEM_B_DQ<55>	MEM_B_DQ<55> - @k2_lib.K2	17B4 32A3
MEM_B_DQ<56>	MEM_B_DQ<56> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<61..56>	MEM_B_DQ<61..56> - @k2_lib.K2	102C1
MEM_B_DQ<57>	MEM_B_DQ<57> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<58>	MEM_B_DQ<58> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<59>	MEM_B_DQ<59> - @k2_lib.K2	17B4 32A6
MEM_B_DQ<60>	MEM_B_DQ<60> - @k2_lib.K2	17A4 32A3
MEM_B_DQ<61>	MEM_B_DQ<61> - @k2_lib.K2	17A4 32A3
MEM_B_DQ<62>	MEM_B_DQ<62> - @k2_lib.K2	7A7 17A4 32A3 102C1
MEM_B_DQ<63>	MEM_B_DQ<63> - @k2_lib.K2	17A4 32A3 102C1
MEM_B_DQS_N<0>	MEM_B_DQS_N<0> - @k2_lib.K2	7A7 17C1 32D6 102B1
MEM_B_DQS_N<1>	MEM_B_DQS_N<1> - @k2_lib.K2	7A7 17C1 32D6 102B1
MEM_B_DQS_N<2>	MEM_B_DQS_N<2> - @k2_lib.K2	7A7 17C1 32C6 102B1
MEM_B_DQS_N<3>	MEM_B_DQS_N<3> - @k2_lib.K2	7A7 17C1 32C3 102B1
MEM_B_DQS_N<4>	MEM_B_DQS_N<4> - @k2_lib.K2	7A7 17C1 32B6 102B1
MEM_B_DQS_N<5>	MEM_B_DQS_N<5> - @k2_lib.K2	7A7 17C1 32B3 102B1
MEM_B_DQS_N<6>	MEM_B_DQS_N<6> - @k2_lib.K2	7A7 17C1 32A6 102B1
MEM_B_DQS_N<7>	MEM_B_DQS_N<7> - @k2_lib.K2	7A7 17C1 32A3 102B1
MEM_B_DQS_P<0>	MEM_B_DQS_P<0> - @k2_lib.K2	7A7 17C1 32D6 102B1
MEM_B_DQS_P<1>	MEM_B_DQS_P<1> - @k2_lib.K2	7A7 17C1 32D6 102B1
MEM_B_DQS_P<2>	MEM_B_DQS_P<2> - @k2_lib.K2	7A7 17C1 32C6 102B1
MEM_B_DQS_P<3>	MEM_B_DQS_P<3> - @k2_lib.K2	7A7 17C1 32C3 102B1
MEM_B_DQS_P<4>	MEM_B_DQS_P<4> - @k2_lib.K2	7A7 17C1 32B6 102B1
MEM_B_DQS_P<5>	MEM_B_DQS_P<5> - @k2_lib.K2	7A7 17C1 32B3 102B1
MEM_B_DQS_P<6>	MEM_B_DQS_P<6> - @k2_lib.K2	7A7 17C1 32A6 102B1
MEM_B_DQS_P<7>	MEM_B_DQS_P<7> - @k2_lib.K2	7A7 17C1 32A3 102B1
MEM_B_RAS_L	MEM_B_RAS_L - @k2_lib.K2	17B1 32B3 33A6 102D1
MEM_B_SA<0>	MEM_B_SA<0> - @k2_lib.K2	32A4
MEM_B_SA<1>	MEM_B_SA<1> - @k2_lib.K2	32A4
MEM_B_WE_L	MEM_B_WE_L - @k2_lib.K2	17B1 32B6 33A6 102D1
MEM_CKE<0>	MEM_CKE<0> - @k2_lib.K2	16D3 31C6 33D6
MEM_CKE<1..0>	MEM_CKE<1..0> - @k2_lib.K2	102D3
MEM_CKE<1>	MEM_CKE<1> - @k2_lib.K2	16D3 31C3 33D6
MEM_CKE<3>	MEM_CKE<3> - @k2_lib.K2	16D3 32C6 33D6
MEM_CKE<4..3>	MEM_CKE<4..3> - @k2_lib.K2	102D1
MEM_CKE<4>	MEM_CKE<4> - @k2_lib.K2	16D3 32C3 33D6
MEM_CLK_N<0>	MEM_CLK_N<0> - @k2_lib.K2	16D3 31D3
MEM_CLK_N<1..0>	MEM_CLK_N<1..0> - @k2_lib.K2	102D3
MEM_CLK_N<1>	MEM_CLK_N<1> - @k2_lib.K2	16D3 31A3
MEM_CLK_N<3>	MEM_CLK_N<3> - @k2_lib.K2	16D3 32D3
MEM_CLK_N<4..3>	MEM_CLK_N<4..3> - @k2_lib.K2	102D1
MEM_CLK_N<4>	MEM_CLK_N<4> - @k2_lib.K2	16D3 32A3
MEM_CLK_P<0>	MEM_CLK_P<0> - @k2_lib.K2	16D3 31D3
MEM_CLK_P<1..0>	MEM_CLK_P<1..0> - @k2_lib.K2	102D3
MEM_CLK_P<1>	MEM_CLK_P<1> - @k2_lib.K2	16D3 31A3
MEM_CLK_P<3>	MEM_CLK_P<3> - @k2_lib.K2	16D3 32D3
MEM_CLK_P<4..3>	MEM_CLK_P<4..3> - @k2_lib.K2	102D1
MEM_CLK_P<4>	MEM_CLK_P<4> - @k2_lib.K2	16D3 32A3
MEM_CS_L<0>	MEM_CS_L<0> - @k2_lib.K2	16D3 31B3 33D6
MEM_CS_L<1..0>	MEM_CS_L<1..0> - @k2_lib.K2	102D3
MEM_CS_L<1>	MEM_CS_L<1> - @k2_lib.K2	16D3 31B6 33D6
MEM_CS_L<2>	MEM_CS_L<2> - @k2_lib.K2	16D3 32B3 33D6
MEM_CS_L<3..2>	MEM_CS_L<3..2> - @k2_lib.K2	102D1
MEM_CS_L<3>	MEM_CS_L<3> - @k2_lib.K2	16C3 32B6 33D6
MEM_ODT<0>	MEM_ODT<0> - @k2_lib.K2	16C3 31B3 33C6
MEM_ODT<1..0>	MEM_ODT<1..0> - @k2_lib.K2	102D3
MEM_ODT<1>	MEM_ODT<1> - @k2_lib.K2	16C3 31B6 33C6
MEM_ODT<2>	MEM_ODT<2> - @k2_lib.K2	16C3 32B3 33C6
MEM_ODT<3..2>	MEM_ODT<3..2> - @k2_lib.K2	102D1
MEM_ODT<3>	MEM_ODT<3> - @k2_lib.K2	16C3 32B6 33C6
MEM_RCOMP	MEM_RCOMP - @k2_lib.K2	16C4
MEM_RCOMP_L	MEM_RCOMP_L - @k2_lib.K2	16C4
MEM_RCOMP_VOH	MEM_RCOMP_VOH - @k2_lib.K2	16C4
MEM_RCOMP_VOL	MEM_RCOMP_VOL - @k2_lib.K2	16C4
MINI_RESET_L	MINI_RESET_L - @k2_lib.K2	28D1 34C3
MXM_DETECT_L	MXM_DETECT_L - @k2_lib.K2	85C4
MXM_PIN170	MXM_PIN170 - @k2_lib.K2	85B5
MXM_PWRSRC_SENSOR_N	MXM_PWRSRC_SENSOR_N - @k2_lib.K2	53C4
MXM_PWRSRC_SENSOR_P	MXM_PWRSRC_SENSOR_P - @k2_lib.K2	53C4
MXM_ROM_WP	MXM_ROM_WP - @k2_lib.K2	85C3
NB_BSEL<0>	NB_BSEL<0> - @k2_lib.K2	13C6 16C6 30C8 100B3
NB_BSEL<1>	NB_BSEL<1> - @k2_lib.K2	13C6 16C6 30B8 100B3
NB_BSEL<2>	NB_BSEL<2> - @k2_lib.K2	13C3 16B6 30B8 100A3
NB_CFG<3>	NB_CFG<3> - @k2_lib.K2	7B3 13C3 16B6
NB_CFG<4>	NB_CFG<4> - @k2_lib.K2	7B3 13C6 16B6
NB_CFG<5>	NB_CFG<5> - @k2_lib.K2	7B3 13C6 16B6 16D7
NB_CFG<6>	NB_CFG<6> - @k2_lib.K2	7B3 13C6 16B6
NB_CFG<7>	NB_CFG<7> - @k2_lib.K2	7B3 13C6 16B6
NB_CFG<8>	NB_CFG<8> - @k2_lib.K2	13C3 16B6
NB_CFG<9>	NB_CFG<9> - @k2_lib.K2	16B6 16D7
NB_CFG<16>	NB_CFG<16> - @k2_lib.K2	16B6 16D7
NB_CFG<19>	NB_CFG<19> - @k2_lib.K2	7C3 16B6 16C7
NB_CFG<20>	NB_CFG<20> - @k2_lib.K2	16B6 16C7
NB_CLINK_VREF	NB_CLINK_VREF - @k2_lib.K2	16A4 104B3
NB_CLKREQ_L	NB_CLKREQ_L - @k2_lib.K2	16A3 29B3 30C2
NB_FSB_RCOMP	NB_FSB_RCOMP - @k2_lib.K2	14A5
NB_FSB_SCOMP	NB_FSB_SCOMP - @k2_lib.K2	14A5
NB_FSB_SCOMP_L	NB_FSB_SCOMP_L - @k2_lib.K2	14A5
NB_FSB_SWING	NB_FSB_SWING - @k2_lib.K2	14A5
NB_FSB_VREF	NB_FSB_VREF - @k2_lib.K2	14A5
NB_RESET_L	NB_RESET_L - @k2_lib.K2	7C7 16B6 28D1
NB_SB_SYNC_L	NB_SB_SYNC_L - @k2_lib.K2	16A3 25B5
NB_TEST1	NB_TEST1 - @k2_lib.K2	16A4
NB_TEST2	NB_TEST2 - @k2_lib.K2	16A4
NB_VCCSM_LF1	NB_VCCSM_LF1 - @k2_lib.K2	18A6
NB_VCCSM_LF2	NB_VCCSM_LF2 - @k2_lib.K2	18A6
NB_VCCSM_LF3	NB_VCCSM_LF3 - @k2_lib.K2	18A6
NB_VCCSM_LF4	NB_VCCSM_LF4 - @k2_lib.K2	18A6
NB_VCCSM_LF5	NB_VCCSM_LF5 - @k2_lib.K2	18A6
NB_VCCSM_LF6	NB_VCCSM_LF6 - @k2_lib.K2	18A6
NB_VCCSM_LF7	NB_VCCSM_LF7 - @k2_lib.K2	18A6
NB_VTTLF_CAP1	NB_VTTLF_CAP1 - @k2_lib.K2	19A4
NB_VTTLF_CAP2	NB_VTTLF_CAP2 - @k2_lib.K2	19A4
NB_VTTLF_CAP3	NB_VTTLF_CAP3 - @k2_lib.K2	19A4
NC_SMC_BATT_CHG_EN	NC_SMC_BATT_CHG_EN - @k2_lib.K2	50D3
	SMC_BATT_CHG_EN - @k2_lib.K2	49C8 50D5
NC_SMC_BATT_ISET	NC_SMC_BATT_ISET - @k2_lib.K2	50D3
	SMC_BATT_ISET - @k2_lib.K2	49B5 50D5
NC_SMC_BATT_TRICKLE_EN_L	NC_SMC_BATT_TRICKLE_EN_L - @k2_lib.K2	50D3
	SMC_BATT_TRICKLE_EN_L - @k2_lib.K2	49C8 50D5
NC_SMC_BATT_VSET	NC_SMC_BATT_VSET - @k2_lib.K2	50D3
	SMC_BATT_VSET - @k2_lib.K2	49B5 50D5
NC_SMC_NB_1V8_ISENSE	NC_SMC_NB_1V8_ISENSE - @k2_lib.K2	50B3
	SMC_NB_1V8_ISENSE - @k2_lib.K2	49A8 50B5
NC_SMC_NB_CORE_ISENSE	NC_SMC_NB_CORE_ISENSE - @k2_lib.K2	50B3
	SMC_NB_CORE_ISENSE - @k2_lib.K2	49A8 50B5
NC_SMC_SYS_ISET	NC_SMC_SYS_ISET - @k2_lib.K2	50D3
	SMC_SYS_ISET - @k2_lib.K2	49B5 50D5
NC_SMC_SYS_VSET	NC_SMC_SYS_VSET - @k2_lib.K2	50D3
	SMC_SYS_VSET - @k2_lib.K2	49B5 50D5
ODD_PWR_EN_L	ODD_PWR_EN_L - @k2_lib.K2	24A4 24A6
ODD_RST_5VTOL_L	ODD_RST_5VTOL_L - @k2_lib.K2	7B3 24B6 44C6 103D3
ODD_THRMD_N	ODD_THRMD_N - @k2_lib.K2	55A5 55B6 108A3
ODD_THRMD_P	ODD_THRMD_P - @k2_lib.K2	55B5 55B6 108A3
P1V8S0_EN_L	P1V8S0_EN_L - @k2_lib.K2	78B7
P1V8S0_EN_L_RC	P1V8S0_EN_L_RC - @k2_lib.K2	78B6
P1V8S0_GDRV	P1V8S0_GDRV - @k2_lib.K2	78B7
P1V8S0_SS	P1V8S0_SS - @k2_lib.K2	78B6
P1V8S0_SS_RC	P1V8S0_SS_RC - @k2_lib.K2	78B7
P2V5S0_SW	P2V5S0_SW - @k2_lib.K2	108D1
P3V3S0_EN_L	P3V3S0_EN_L - @k2_lib.K2	78B3
P3V3S0_SS	P3V3S0_SS - @k2_lib.K2	78B2
P3V3S5_FB	P3V3S5_FB - @k2_lib.K2	77D5
P3V3S5_SW	P3V3S5_SW - @k2_lib.K2	77D5 108D1
P5VREG_FCB	P5VREG_FCB - @k2_lib.K2	76A3 76B5
P5VREG_FSEL	P5VREG_FSEL - @k2_lib.K2	76A2 76B4
P5VS0_EN_L	P5VS0_EN_L - @k2_lib.K2	78D3
P5VS0_SS	P5VS0_SS - @k2_lib.K2	78D2
P5VS3_EN_L	P5VS3_EN_L - @k2_lib.K2	78D7
P5VS3_SS	P5VS3_SS - @k2_lib.K2	78D6
P5VS5_EN	P5VS5_EN - @k2_lib.K2	77D6

PANEL_ID	PANEL_ID - @k2_lib.K2	28B2
	TP_SB_GPIO20 - @k2_lib.K2	25C5 28B1
PCIE_ENET_D2R_C_N	PCIE_ENET_D2R_C_N - @k2_lib.K2	37C4 108C3
PCIE_ENET_D2R_C_P	PCIE_ENET_D2R_C_P - @k2_lib.K2	37C4 108C3
PCIE_ENET_D2R_N	PCIE_ENET_D2R_N - @k2_lib.K2	7B8 24C5 37C8 104C3
PCIE_ENET_D2R_P	PCIE_ENET_D2R_P - @k2_lib.K2	7B8 24C5 37C8 104C3
PCIE_ENET_R2D_C_N	PCIE_ENET_R2D_C_N - @k2_lib.K2	24C5 37C8 104C3
PCIE_ENET_R2D_C_P	PCIE_ENET_R2D_C_P - @k2_lib.K2	24C5 37C8 104C3
PCIE_ENET_R2D_N	PCIE_ENET_R2D_N - @k2_lib.K2	7D6 37C4 108C3
PCIE_ENET_R2D_P	PCIE_ENET_R2D_P - @k2_lib.K2	7D6 37C4 108C3
PCIE_FW_D2R_C_N	PCIE_FW_D2R_C_N - @k2_lib.K2	40C3 108C3
PCIE_FW_D2R_C_P	PCIE_FW_D2R_C_P - @k2_lib.K2	40C3 108C3
PCIE_FW_D2R_N	PCIE_FW_D2R_N - @k2_lib.K2	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_N - @k2_lib.K2	24D5 42A2
PCIE_FW_D2R_P	PCIE_FW_D2R_P - @k2_lib.K2	7B8 40C2 42A3 104C3
	TP_PCIE_FW_D2R_P - @k2_lib.K2	24D5 42A2
PCIE_FW_R2D_C_N	PCIE_FW_R2D_C_N - @k2_lib.K2	40C1 42A2 104C3
	TP_PCIE_FW_R2D_C_N - @k2_lib.K2	24D5 42A3
PCIE_FW_R2D_C_P	PCIE_FW_R2D_C_P - @k2_lib.K2	40C1 42A2 104C3
	TP_PCIE_FW_R2D_C_P - @k2_lib.K2	24D5 42A3
PCIE_FW_R2D_N	PCIE_FW_R2D_N - @k2_lib.K2	7D6 40C3 108C3
PCIE_FW_R2D_P	PCIE_FW_R2D_P - @k2_lib.K2	7D6 40C3 108C3
PCIE_MINI_D2R_N	PCIE_MINI_D2R_N - @k2_lib.K2	7B8 24D5 34C8 104C3
PCIE_MINI_D2R_P	PCIE_MINI_D2R_P - @k2_lib.K2	7B8 24C5 34C8 104C3
PCIE_MINI_R2D_C_N	PCIE_MINI_R2D_C_N - @k2_lib.K2	24C5 34B8 104C3
PCIE_MINI_R2D_C_P	PCIE_MINI_R2D_C_P - @k2_lib.K2	24C5 34B8 104C3
PCIE_MINI_R2D_N	PCIE_MINI_R2D_N - @k2_lib.K2	34B6 108C3
PCIE_MINI_R2D_P	PCIE_MINI_R2D_P - @k2_lib.K2	34B6 108B3
PCIE_WAKE_L	PCIE_WAKE_L - @k2_lib.K2	25C8 34C6 37B8
PCI_AD<0>	PCI_AD<0> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_0 - @k2_lib.K2	28C4
PCI_AD<18..0>	PCI_AD<18..0> - @k2_lib.K2	104D3
	TP_PCI_AD_18 - @k2_lib.K2	28B4
PCI_AD<1>	PCI_AD<1> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_1 - @k2_lib.K2	28C4
PCI_AD<2>	PCI_AD<2> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_2 - @k2_lib.K2	28C4
PCI_AD<3>	PCI_AD<3> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_3 - @k2_lib.K2	28C4
PCI_AD<4>	PCI_AD<4> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_4 - @k2_lib.K2	7D2 28C4
PCI_AD<5>	PCI_AD<5> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_5 - @k2_lib.K2	28C4
PCI_AD<6>	PCI_AD<6> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_6 - @k2_lib.K2	28C4
PCI_AD<7>	PCI_AD<7> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_7 - @k2_lib.K2	28C4
PCI_AD<8>	PCI_AD<8> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_8 - @k2_lib.K2	28C4
PCI_AD<9>	PCI_AD<9> - @k2_lib.K2	24B8 28C5
	TP_PCI_AD_9 - @k2_lib.K2	28C4
PCI_AD<10>	PCI_AD<10> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_10 - @k2_lib.K2	28C4
PCI_AD<11>	PCI_AD<11> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_11 - @k2_lib.K2	28C4
PCI_AD<12>	PCI_AD<12> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_12 - @k2_lib.K2	28C4
PCI_AD<13>	PCI_AD<13> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_13 - @k2_lib.K2	28C4
PCI_AD<14>	PCI_AD<14> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_14 - @k2_lib.K2	28C4
PCI_AD<15>	PCI_AD<15> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_15 - @k2_lib.K2	28C4
PCI_AD<16>	PCI_AD<16> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_16 - @k2_lib.K2	28C4
PCI_AD<17>	PCI_AD<17> - @k2_lib.K2	24A8 28C5
	TP_PCI_AD_17 - @k2_lib.K2	28C4
PCI_AD<18>	PCI_AD<18> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_18 - @k2_lib.K2	28B4
PCI_AD<19>	PCI_AD<19> - @k2_lib.K2	24A8 28B5 104D3
	TP_PCI_AD_19 - @k2_lib.K2	28B4
PCI_AD<20>	PCI_AD<20> - @k2_lib.K2	24A8 28B5 104D3
	TP_PCI_AD_20 - @k2_lib.K2	28B4
PCI_AD<21>	PCI_AD<21> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_21 - @k2_lib.K2	28B4
PCI_AD<31..21>	PCI_AD<31..21> - @k2_lib.K2	104D3
	TP_PCI_AD_31 - @k2_lib.K2	28B4
PCI_AD<22>	PCI_AD<22> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_22 - @k2_lib.K2	28B4
PCI_AD<23>	PCI_AD<23> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_23 - @k2_lib.K2	28B4
PCI_AD<24>	PCI_AD<24> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_24 - @k2_lib.K2	28B4
PCI_AD<25>	PCI_AD<25> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_25 - @k2_lib.K2	28B4
PCI_AD<26>	PCI_AD<26> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_26 - @k2_lib.K2	28B4
PCI_AD<27>	PCI_AD<27> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_27 - @k2_lib.K2	28B4
PCI_AD<28>	PCI_AD<28> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_28 - @k2_lib.K2	28B4
PCI_AD<29>	PCI_AD<29> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_29 - @k2_lib.K2	28B4
PCI_AD<30>	PCI_AD<30> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_30 - @k2_lib.K2	28B4
PCI_AD<31>	PCI_AD<31> - @k2_lib.K2	24A8 28B5
	TP_PCI_AD_31 - @k2_lib.K2	28B4
PCI_CLK33M_LPCPLUS	PCI_CLK33M_LPCPLUS - @k2_lib.K2	7D4 30A3 51C4 105C3
PCI_CLK33M_SB	PCI_CLK33M_SB - @k2_lib.K2	7B8 24A6 30A3 105B3
PCI_CLK33M_SMC	PCI_CLK33M_SMC - @k2_lib.K2	7C6 30A3 49C8 105B3
PCI_CLK33M_TPM	PCI_CLK33M_TPM - @k2_lib.K2	105B3
PCI_C_BE_L<0>	PCI_C_BE_L<0> - @k2_lib.K2	24B6 28B5
	TP_PCI_C_BE_L_0 - @k2_lib.K2	28B4
PCI_C_BE_L<3..0>	PCI_C_BE_L<3..0> - @k2_lib.K2	104D3
	TP_PCI_C_BE_L_3 - @k2_lib.K2	28B4
PCI_C_BE_L<1>	PCI_C_BE_L<1> - @k2_lib.K2	24A6 28B5
	TP_PCI_C_BE_L_1 - @k2_lib.K2	28B4
PCI_C_BE_L<2>	PCI_C_BE_L<2> - @k2_lib.K2	24A6 28B5
	TP_PCI_C_BE_L_2 - @k2_lib.K2	28B4
PCI_C_BE_L<3>	PCI_C_BE_L<3> - @k2_lib.K2	24A6 28B5
	TP_PCI_C_BE_L_3 - @k2_lib.K2	28B4
PCI_DEVSEL_L	PCI_DEVSEL_L - @k2_lib.K2	24A4 24A6 104D3
PCI_FRAME_L	PCI_FRAME_L - @k2_lib.K2	24A4 24A6 104D3
PCI_FW_GNT_L	PCI_FW_GNT_L - @k2_lib.K2	24B5 104D3
	BOOT_LPC_SPI_L - @k2_lib.K2	7D4 24B5 51B6
PCI_FW_REQ_L	PCI_FW_REQ_L - @k2_lib.K2	24A4 24B6 104D3
PCI_GNT1_L	PCI_GNT1_L - @k2_lib.K2	104D3
PCI_GNT2_L	PCI_GNT2_L - @k2_lib.K2	104C3
PCI_IRDY_L	PCI_IRDY_L - @k2_lib.K2	24A4 24A6 104D3
PCI_LOCK_L	PCI_LOCK_L - @k2_lib.K2	24A4 24A6 104D3
PCI_PAR	PCI_PAR - @k2_lib.K2	24A6 28B5 104D3
	TP_PCI_PAR - @k2_lib.K2	28B4
PCI_PERR_L	PCI_PERR_L - @k2_lib.K2	24A4 24A6 104D3
PCI_PME_FW_L	PCI_PME_FW_L - @k2_lib.K2	25B5 25C5 40C3

PCI_REQ1_L	PCI_REQ1_L - @k2_lib.K2	7C3 24A4 24B6 104D3
PCI_REQ2_L	PCI_REQ2_L - @k2_lib.K2	7C3 24A4 24B6 104D3
PCI_RST_L	PCI_RST_L - @k2_lib.K2	24A6 28B5
	TP_PCI_RST_L - @k2_lib.K2	28B4
PCI_SERR_L	PCI_SERR_L - @k2_lib.K2	7D2 24A4 24A6 28C4 104D3
PCI_STOP_L	PCI_STOP_L - @k2_lib.K2	24A4 24A6 104D3
PCI_TRDY_L	PCI_TRDY_L - @k2_lib.K2	24A4 24A6 104D3
PEG_COMP	PEG_COMP - @k2_lib.K2	15D3
PEG_D2R_N<0>	PEG_D2R_N<0> - @k2_lib.K2	15D3 84C4
PEG_D2R_N<6..0>	PEG_D2R_N<6..0> - @k2_lib.K2	101D3
PEG_D2R_N<1>	PEG_D2R_N<1> - @k2_lib.K2	15D3 84C4
PEG_D2R_N<2>	PEG_D2R_N<2> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<3>	PEG_D2R_N<3> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<4>	PEG_D2R_N<4> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<5>	PEG_D2R_N<5> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<6>	PEG_D2R_N<6> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<7>	PEG_D2R_N<7> - @k2_lib.K2	7A7 15D3 84B4 101D3
PEG_D2R_N<8>	PEG_D2R_N<8> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<15..8>	PEG_D2R_N<15..8> - @k2_lib.K2	101D3
PEG_D2R_N<9>	PEG_D2R_N<9> - @k2_lib.K2	15D3 84B4
PEG_D2R_N<10>	PEG_D2R_N<10> - @k2_lib.K2	15C3 84B4
PEG_D2R_N<11>	PEG_D2R_N<11> - @k2_lib.K2	15C3 84A4
PEG_D2R_N<12>	PEG_D2R_N<12> - @k2_lib.K2	15C3 84A4
PEG_D2R_N<13>	PEG_D2R_N<13> - @k2_lib.K2	15C3 84A4
PEG_D2R_N<14>	PEG_D2R_N<14> - @k2_lib.K2	15C3 84A4
PEG_D2R_N<15>	PEG_D2R_N<15> - @k2_lib.K2	15C3 84A4
PEG_D2R_P<0>	PEG_D2R_P<0> - @k2_lib.K2	15C3 84C4
PEG_D2R_P<6..0>	PEG_D2R_P<6..0> - @k2_lib.K2	101D3
PEG_D2R_P<1>	PEG_D2R_P<1> - @k2_lib.K2	15C3 84C4
PEG_D2R_P<2>	PEG_D2R_P<2> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<3>	PEG_D2R_P<3> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<4>	PEG_D2R_P<4> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<5>	PEG_D2R_P<5> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<6>	PEG_D2R_P<6> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<7>	PEG_D2R_P<7> - @k2_lib.K2	7A7 15C3 84B4 101D3
PEG_D2R_P<8>	PEG_D2R_P<8> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<15..8>	PEG_D2R_P<15..8> - @k2_lib.K2	101D3
PEG_D2R_P<9>	PEG_D2R_P<9> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<10>	PEG_D2R_P<10> - @k2_lib.K2	15C3 84B4
PEG_D2R_P<11>	PEG_D2R_P<11> - @k2_lib.K2	15C3 84A4
PEG_D2R_P<12>	PEG_D2R_P<12> - @k2_lib.K2	15C3 84A4
PEG_D2R_P<13>	PEG_D2R_P<13> - @k2_lib.K2	15C3 84A4
PEG_D2R_P<14>	PEG_D2R_P<14> - @k2_lib.K2	15C3 84A4
PEG_D2R_P<15>	PEG_D2R_P<15> - @k2_lib.K2	15C3 84A4
PEG_R2D_C_N<0>	PEG_R2D_C_N<0> - @k2_lib.K2	15C3 84C8
PEG_R2D_C_N<15..0>	PEG_R2D_C_N<15..0> - @k2_lib.K2	101D3
PEG_R2D_C_N<1>	PEG_R2D_C_N<1> - @k2_lib.K2	15C3 84C8
PEG_R2D_C_N<2>	PEG_R2D_C_N<2> - @k2_lib.K2	15C3 84B8
PEG_R2D_C_N<3>	PEG_R2D_C_N<3> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<4>	PEG_R2D_C_N<4> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<5>	PEG_R2D_C_N<5> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<6>	PEG_R2D_C_N<6> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<7>	PEG_R2D_C_N<7> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<8>	PEG_R2D_C_N<8> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<9>	PEG_R2D_C_N<9> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_N<10>	PEG_R2D_C_N<10> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_N<11>	PEG_R2D_C_N<11> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_N<12>	PEG_R2D_C_N<12> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_N<13>	PEG_R2D_C_N<13> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_N<14>	PEG_R2D_C_N<14> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_N<15>	PEG_R2D_C_N<15> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_P<0>	PEG_R2D_C_P<0> - @k2_lib.K2	15B3 84C8
PEG_R2D_C_P<15..0>	PEG_R2D_C_P<15..0> - @k2_lib.K2	101D3
PEG_R2D_C_P<1>	PEG_R2D_C_P<1> - @k2_lib.K2	15B3 84C8
PEG_R2D_C_P<2>	PEG_R2D_C_P<2> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<3>	PEG_R2D_C_P<3> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<4>	PEG_R2D_C_P<4> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<5>	PEG_R2D_C_P<5> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<6>	PEG_R2D_C_P<6> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<7>	PEG_R2D_C_P<7> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<8>	PEG_R2D_C_P<8> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<9>	PEG_R2D_C_P<9> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<10>	PEG_R2D_C_P<10> - @k2_lib.K2	15B3 84B8
PEG_R2D_C_P<11>	PEG_R2D_C_P<11> - @k2_lib.K2	15B3 84A8
PEG_R2D_C_P<12>	PEG_R2D_C_P<12> - @k2_lib.K2	15A3 84A8
PEG_R2D_C_P<13>	PEG_R2D_C_P<13> - @k2_lib.K2	15A3 84A8
PEG_R2D_C_P<14>	PEG_R2D_C_P<14> - @k2_lib.K2	15A3 84A8
PEG_R2D_C_P<15>	PEG_R2D_C_P<15> - @k2_lib.K2	15A3 84A8
PEG_R2D_N<0>	PEG_R2D_N<0> - @k2_lib.K2	84A7
PEG_R2D_N<15..0>	PEG_R2D_N<15..0> - @k2_lib.K2	101D3
PEG_R2D_N<1>	PEG_R2D_N<1> - @k2_lib.K2	84A7
PEG_R2D_N<2>	PEG_R2D_N<2> - @k2_lib.K2	84A7
PEG_R2D_N<3>	PEG_R2D_N<3> - @k2_lib.K2	84A7
PEG_R2D_N<4>	PEG_R2D_N<4> - @k2_lib.K2	84A7
PEG_R2D_N<5>	PEG_R2D_N<5> - @k2_lib.K2	84A7
PEG_R2D_N<6>	PEG_R2D_N<6> - @k2_lib.K2	84B7
PEG_R2D_N<7>	PEG_R2D_N<7> - @k2_lib.K2	84B7
PEG_R2D_N<8>	PEG_R2D_N<8> - @k2_lib.K2	84B7
PEG_R2D_N<9>	PEG_R2D_N<9> - @k2_lib.K2	84B7
PEG_R2D_N<10>	PEG_R2D_N<10> - @k2_lib.K2	84B7
PEG_R2D_N<11>	PEG_R2D_N<11> - @k2_lib.K2	84B7
PEG_R2D_N<12>	PEG_R2D_N<12> - @k2_lib.K2	84B7
PEG_R2D_N<13>	PEG_R2D_N<13> - @k2_lib.K2	84B7
PEG_R2D_N<14>	PEG_R2D_N<14> - @k2_lib.K2	84C7
PEG_R2D_N<15>	PEG_R2D_N<15> - @k2_lib.K2	84C7
PEG_R2D_P<0>	PEG_R2D_P<0> - @k2_lib.K2	84A7
PEG_R2D_P<15..0>	PEG_R2D_P<15..0> - @k2_lib.K2	101D3
PEG_R2D_P<1>	PEG_R2D_P<1> - @k2_lib.K2	84A7
PEG_R2D_P<2>	PEG_R2D_P<2> - @k2_lib.K2	84A7
PEG_R2D_P<3>	PEG_R2D_P<3> - @k2_lib.K2	84A7
PEG_R2D_P<4>	PEG_R2D_P<4> - @k2_lib.K2	84A7
PEG_R2D_P<5>	PEG_R2D_P<5> - @k2_lib.K2	84B7
PEG_R2D_P<6>	PEG_R2D_P<6> - @k2_lib.K2	84B7
PEG_R2D_P<7>	PEG_R2D_P<7> - @k2_lib.K2	84B7
PEG_R2D_P<8>	PEG_R2D_P<8> - @k2_lib.K2	84B7
PEG_R2D_P<9>	PEG_R2D_P<9> - @k2_lib.K2	84B7
PEG_R2D_P<10>	PEG_R2D_P<10> - @k2_lib.K2	84B7
PEG_R2D_P<11>	PEG_R2D_P<11> - @k2_lib.K2	84B7
PEG_R2D_P<12>	PEG_R2D_P<12> - @k2_lib.K2	84B7
PEG_R2D_P<13>	PEG_R2D_P<13> - @k2_lib.K2	84B7
PEG_R2D_P<14>	PEG_R2D_P<14> - @k2_lib.K2	84C7
PEG_R2D_P<15>	PEG_R2D_P<15> - @k2_lib.K2	84C7
PEG_RESET_L	PEG_RESET_L - @k2_lib.K2	28C1 85C7
PGOOD_0V9_S0	PGOOD_0V9_S0 - @k2_lib.K2	70C4 70C4
PGOOD_1V05_S0	PGOOD_1V05_S0 - @k2_lib.K2	70B4 73B3
PGOOD_1V5_S0	PGOOD_1V5_S0 - @k2_lib.K2	70B4 73B5
PGOOD_1V8_S0	PGOOD_1V8_S0 - @k2_lib.K2	70C4 70D4
PGOOD_1V8_S3	PGOOD_1V8_S3 - @k2_lib.K2	70D4 75C8
PGOOD_1V25_S0	PGOOD_1V25_S0 - @k2_lib.K2	70B4 74B5
PGOOD_3V3_S0	PGOOD_3V3_S0 - @k2_lib.K2	70C8 70D4
PGOOD_3V3_S3	PGOOD_3V3_S3 - @k2_lib.K2	70D4 76B4
PGOOD_3V3_S5	PGOOD_3V3_S5 - @k2_lib.K2	70B4 77D4
	RSMRST_PWRGD - @k2_lib.K2	49D8 70B2
PGOOD_5V_S0	PGOOD_5V_S0 - @k2_lib.K2	70C4 70C4

PGOOD_5V_S3_L	PGOOD_5V_S3_L - @k2_lib.K2	76A6
PGOOD_12V_S0	PGOOD_12V_S0 - @k2_lib.K2	70B8 76D5
PGOOD_CR_S0	PGOOD_CR_S0 - @k2_lib.K2	70C7
PGOOD_MCH_CORE_S0	PGOOD_MCH_CORE_S0 - @k2_lib.K2	70B4 74B3
PGOOD_S0_OUT1	PGOOD_S0_OUT1 - @k2_lib.K2	70C3
PLT_RST_L	PLT_RST_L - @k2_lib.K2	24A6 28D4
PM_BATLOW_L	PM_BATLOW_L - @k2_lib.K2	25A5 25C3 49B8
PM_BMBUSY_L	PM_BMBUSY_L - @k2_lib.K2	16B6 25D5
PM_CLKRUN_L	PM_CLKRUN_L - @k2_lib.K2	7B8 7D4 25C8 49C5 51B6
PM_DPRSLPVR	PM_DPRSLPVR - @k2_lib.K2	16A6 25C3 71C8 100B3
PM_EXTTS_L<0>	PM_EXTTS_L<0> - @k2_lib.K2	16B7 31C3 49B8
PM_EXTTS_L<1>	PM_EXTTS_L<1> - @k2_lib.K2	16B7 32C3 49B8
PM_LAN_ENABLE	PM_LAN_ENABLE - @k2_lib.K2	25C2 49D8
PM_LATRIGGER_L	PM_LATRIGGER_L - @k2_lib.K2	13C3 24C8
PM_PWRBTN_L	PM_PWRBTN_L - @k2_lib.K2	25C3 49C8
PM_RI_L	PM_RI_L - @k2_lib.K2	25A5 25D5
PM_RSMRST_L	PM_RSMRST_L - @k2_lib.K2	25C2 49C8
PM_S4_STATE_L	PM_S4_STATE_L - @k2_lib.K2	7C4 7D3 25D3 46C8 49C4 75D8 78D7
PM_S4_STATE_L_SMC	PM_S4_STATE_L_SMC - @k2_lib.K2	49C6
PM_SLP_S3_L	PM_SLP_S3_L - @k2_lib.K2	6D8 7C4 25D3 49C4 70A8 75A5 78B4 78B7 78D4
PM_SLP_S3_L_SMC	PM_SLP_S3_L_SMC - @k2_lib.K2	49C6
PM_SLP_S3_OD	PM_SLP_S3_OD - @k2_lib.K2	6D7
PM_SLP_S5_L	PM_SLP_S5_L - @k2_lib.K2	25D3 49C5 50A2
PM_STPCPU_L	PM_STPCPU_L - @k2_lib.K2	25C8 29C3 30C2
PM_STPPCI_L	PM_STPPCI_L - @k2_lib.K2	25C8 29C3 30C2
PM_SUS_STAT_L	PM_SUS_STAT_L - @k2_lib.K2	7C4 7D4 25D5 49C5 50A2 51B4
PM_SYSRST_L	PM_SYSRST_L - @k2_lib.K2	7B8 25D5 28A3 49B8
PM_THRMTRIP_L	PM_THRMTRIP_L - @k2_lib.K2	10C6 16A6 23C2 50C3 100B3
PM_THRM_L	PM_THRM_L - @k2_lib.K2	25C5
POWER_BUTTON_L	POWER_BUTTON_L - @k2_lib.K2	50C7
PP1V0_S5_FW_AVDD	PP1V0_S5_FW_AVDD - @k2_lib.K2	40D3 42A6 42D4
PP1V0_S5_FW_DVDD	PP1V0_S5_FW_DVDD - @k2_lib.K2	40D6 42B8 42C4
PP1V05_S0_NB_VCCPEG	PP1V05_S0_NB_VCCPEG - @k2_lib.K2	15D2 19B3 21D3
	PP1V05_S0_NB_VCCRXRDMI - @k2_lib.K2	19B3 21C3
PP1V5_S0_NB_VCCD_TVDAC	PP1V5_S0_NB_VCCD_TVDAC - @k2_lib.K2	19B6 22B1
PP1V5_S0_SB_VCCDMIPLL	PP1V5_S0_SB_VCCDMIPLL - @k2_lib.K2	26C3 27A6
PP1V5_S0_SB_VCCDMIPLL_F	PP1V5_S0_SB_VCCDMIPLL_F - @k2_lib.K2	27A8
PP1V5_S0_SB_VCCSATAPLL	PP1V5_S0_SB_VCCSATAPLL - @k2_lib.K2	26B6 27A6
PP1V5_S0_SB_VCCSATAPLL_F	PP1V5_S0_SB_VCCSATAPLL_F - @k2_lib.K2	27A8
PP1V8_S3M_NB_VCCSMCK	PP1V8_S3M_NB_VCCSMCK - @k2_lib.K2	19B3 21A2
PP1V8_S3M_NB_VCCSMCK_RC	PP1V8_S3M_NB_VCCSMCK_RC - @k2_lib.K2	21A4
PP1V8_S3_R	PP1V8_S3_R - @k2_lib.K2	75C1
PP1V9_ENET_CTAP	PP1V9_ENET_CTAP - @k2_lib.K2	39D7
PP1V9_ENET_PHY_AVDD	PP1V9_ENET_PHY_AVDD - @k2_lib.K2	37C6 104B3
PP1V9_S3_ENET	PP1V9_S3_ENET - @k2_lib.K2	37C7 38C3 39D8
PP1V25_S0M_NB_MPLL_RC	PP1V25_S0M_NB_MPLL_RC - @k2_lib.K2	21C3
PP1V25_S0M_NB_VCCAXD	PP1V25_S0M_NB_VCCAXD - @k2_lib.K2	16A2 19C3 21A6
PP1V25_S0M_NB_VCCA_HPLL	PP1V25_S0M_NB_VCCA_HPLL - @k2_lib.K2	19D6 21D1
PP1V25_S0M_NB_VCCA_MPLL	PP1V25_S0M_NB_VCCA_MPLL - @k2_lib.K2	19D6 21C1
PP1V25_S0M_NB_VCCA_SM	PP1V25_S0M_NB_VCCA_SM - @k2_lib.K2	19C6 21B5
PP1V25_S0M_NB_VCCA_SM_CK	PP1V25_S0M_NB_VCCA_SM_CK - @k2_lib.K2	19B6 21B5
PP1V25_S0_NB_PEGPLL	PP1V25_S0_NB_PEGPLL - @k2_lib.K2	19C6 21B2
PP1V25_S0_NB_PEGPLL_RC	PP1V25_S0_NB_PEGPLL_RC - @k2_lib.K2	21B4
PP1V25_S0_NB_VCCAXF	PP1V25_S0_NB_VCCAXF - @k2_lib.K2	19C3 21D3
PP3V3_FW_ESD	PP3V3_FW_ESD - @k2_lib.K2	43A6 43A6 43B6 43C5 43D5
PP3V3_G3_SB_RTC	PP3V3_G3_SB_RTC - @k2_lib.K2	23D7 26D6 27D5 28D5
PP3V3_S0M_CK505_VDD48	PP3V3_S0M_CK505_VDD48 - @k2_lib.K2	29D4
PP3V3_S0M_CK505_VDDA	PP3V3_S0M_CK505_VDDA - @k2_lib.K2	29C6
PP3V3_S0M_CK505_VDDA_R	PP3V3_S0M_CK505_VDDA_R - @k2_lib.K2	29C7
PP3V3_S0M_CK505_VDD_CPU_SRC	PP3V3_S0M_CK505_VDD_CPU_SRC - @k2_lib.K2	29D7
PP3V3_S0M_CK505_VDD_PCI	PP3V3_S0M_CK505_VDD_PCI - @k2_lib.K2	29D4
PP3V3_S0M_CK505_VDD_REF	PP3V3_S0M_CK505_VDD_REF - @k2_lib.K2	29C4
PP3V3_S0_CPUTHMSNS_R	PP3V3_S0_CPUTHMSNS_R - @k2_lib.K2	55D4
PP3V3_S0_IMVP6_3V3	PP3V3_S0_IMVP6_3V3 - @k2_lib.K2	71D7
PP3V3_S0_NB1V05_FOLLOW_R	PP3V3_S0_NB1V05_FOLLOW_R - @k2_lib.K2	21C4
PP3V3_S0_NBCORE_FOLLOW_R	PP3V3_S0_NBCORE_FOLLOW_R - @k2_lib.K2	21B4
PP3V3_S3_ENET_O	PP3V3_S3_ENET_O - @k2_lib.K2	38C5
PP3V3_S5_AVREF_SMC	PP3V3_S5_AVREF_SMC - @k2_lib.K2	49D4 50B7
PP3V3_S5_FW_AVDD1	PP3V3_S5_FW_AVDD1 - @k2_lib.K2	40D4 42A8 42B1
PP3V3_S5_FW_AVDD2	PP3V3_S5_FW_AVDD2 - @k2_lib.K2	40D3 42A7 42B1
PP3V3_S5_SMC_AVCC	PP3V3_S5_SMC_AVCC - @k2_lib.K2	49D3
PP5VREG_INTVCC	PP5VREG_INTVCC - @k2_lib.K2	76A2 76A6 76C3 76C6
PP5V_S0_DDC	PP5V_S0_DDC - @k2_lib.K2	94D3 94D4
PP5V_S0_DDC_DIODE	PP5V_S0_DDC_DIODE - @k2_lib.K2	94D6
PP5V_S0_DDC_FUSE	PP5V_S0_DDC_FUSE - @k2_lib.K2	94D5
PP5V_S0_IMVP6_VDD	PP5V_S0_IMVP6_VDD - @k2_lib.K2	71D7
PP5V_S0_SB_V5REF	PP5V_S0_SB_V5REF - @k2_lib.K2	26D6 27C7
PP5V_S3_BNDI	PP5V_S3_BNDI - @k2_lib.K2	47B5 47D5
PP5V_S5_SB_V5REF_SUS	PP5V_S5_SB_V5REF_SUS - @k2_lib.K2	26D6 27D7
PP5V_USB2_PORT0	PP5V_USB2_PORT0 - @k2_lib.K2	46B7
PP5V_USB2_PORT0_F	PP5V_USB2_PORT0_F - @k2_lib.K2	46B5
PP5V_USB2_PORT1	PP5V_USB2_PORT1 - @k2_lib.K2	46C6
PP5V_USB2_PORT1_F	PP5V_USB2_PORT1_F - @k2_lib.K2	46C5
PP5V_USB2_PORT2	PP5V_USB2_PORT2 - @k2_lib.K2	46D6
PP5V_USB2_PORT2_F	PP5V_USB2_PORT2_F - @k2_lib.K2	46D2
PP12V_S0_INPUT	PP12V_S0_INPUT - @k2_lib.K2	6D8 53B5
PP12V_S5_INPUT	PP12V_S5_INPUT - @k2_lib.K2	6D6 53C5
PPVBATT_G3_RTC	PPVBATT_G3_RTC - @k2_lib.K2	28D8
PPVBATT_G3_RTC_R	PPVBATT_G3_RTC_R - @k2_lib.K2	28D7
PPVIN_S5_5VS5_R	PPVIN_S5_5VS5_R - @k2_lib.K2	76C5
PPVIN_S5_IMVP6_VIN	PPVIN_S5_IMVP6_VIN - @k2_lib.K2	71D7
PPV_LCD_CONN	PPV_LCD_CONN - @k2_lib.K2	6A7 90A6 90A8 90C5
PPV_LCD_SW	PPV_LCD_SW - @k2_lib.K2	90C6
PPV_S0_LCD	PPV_S0_LCD - @k2_lib.K2	90C8
PPV_S0_MXM_PWRSRC	PPV_S0_MXM_PWRSRC - @k2_lib.K2	53D3 53D5 84C4
PPV_S3_ENET_O	PPV_S3_ENET_O - @k2_lib.K2	38B5
REMOTE_TEMP_ADDR	REMOTE_TEMP_ADDR - @k2_lib.K2	55A3
REMOTE_THRMD_M	REMOTE_THRMD_M - @k2_lib.K2	55A4
RSVD_EXTGPU_LVDS_EN	RSVD_EXTGPU_LVDS_EN - @k2_lib.K2	25D2
RSVD_MINI_BT_ACTIVE	RSVD_MINI_BT_ACTIVE - @k2_lib.K2	34C6
RSVD_MINI_WLAN_ACTIVE	RSVD_MINI_WLAN_ACTIVE - @k2_lib.K2	34C6

RUNSS_GATE_D_L	RUNSS_GATE_D_L - @k2_lib.K2	70A7 70B7 70B7
SATA_A_D2R_C_N	SATA_A_D2R_C_N - @k2_lib.K2	45D7 103C3
SATA_A_D2R_C_P	SATA_A_D2R_C_P - @k2_lib.K2	45C7 103C3
SATA_A_D2R_N	SATA_A_D2R_N - @k2_lib.K2	7B8 23B6 45C5 103C3
SATA_A_D2R_P	SATA_A_D2R_P - @k2_lib.K2	7B8 23B6 45C5 103D3
SATA_A_R2D_C_N	SATA_A_R2D_C_N - @k2_lib.K2	23B6 45D5 103D3
SATA_A_R2D_C_P	SATA_A_R2D_C_P - @k2_lib.K2	23B6 45D5 103D3
SATA_A_R2D_N	SATA_A_R2D_N - @k2_lib.K2	45D7 103D3
SATA_A_R2D_P	SATA_A_R2D_P - @k2_lib.K2	45D7 103D3
SATA_B_D2R_N	SATA_B_D2R_N - @k2_lib.K2	23B6 45B7 103C3
	TP_SATA_B_D2R_N - @k2_lib.K2	45B6
SATA_B_D2R_P	SATA_B_D2R_P - @k2_lib.K2	23B6 45B7 103C3
	TP_SATA_B_D2R_P - @k2_lib.K2	45B6
SATA_B_DET_L	SATA_B_DET_L - @k2_lib.K2	25D3
SATA_B_PWR_EN_L	SATA_B_PWR_EN_L - @k2_lib.K2	25B5 25C5
SATA_B_R2D_C_N	SATA_B_R2D_C_N - @k2_lib.K2	23B6 45B6 103C3
	TP_SATA_B_R2D_N - @k2_lib.K2	45B7
SATA_B_R2D_C_P	SATA_B_R2D_C_P - @k2_lib.K2	23B6 45B6 103C3
	TP_SATA_B_R2D_P - @k2_lib.K2	45B7
SATA_C_D2R_N	SATA_C_D2R_N - @k2_lib.K2	23B6 45B7
	TP_SATA_C_D2R_N - @k2_lib.K2	45B5
SATA_C_D2R_P	SATA_C_D2R_P - @k2_lib.K2	23B6 45B7
	TP_SATA_C_D2R_P - @k2_lib.K2	45B5
SATA_C_R2D_C_N	SATA_C_R2D_C_N - @k2_lib.K2	23B6 45B6
	TP_SATA_C_R2D_N - @k2_lib.K2	45B7
SATA_C_R2D_C_P	SATA_C_R2D_C_P - @k2_lib.K2	23B6 45B6
	TP_SATA_C_R2D_P - @k2_lib.K2	45B7
SATA_RBIAS	SATA_RBIAS - @k2_lib.K2	45B2 103C3
	SATA_RBIAS_N - @k2_lib.K2	23B6 45B2
	SATA_RBIAS_P - @k2_lib.K2	23A6 45B2
	SATA_RBIAS_N - @k2_lib.K2	23B6 45B2
SB_A20GATE	SB_A20GATE - @k2_lib.K2	23C4
SB_CLINK_VREF0	SB_CLINK_VREF0 - @k2_lib.K2	25C3 104B3
SB_CLINK_VREF1	SB_CLINK_VREF1 - @k2_lib.K2	25C3 104B3
SB_CLK14P3M_TIMER	SB_CLK14P3M_TIMER - @k2_lib.K2	7B8 25D3 30A6 105B3
SB_CLK48M_USBCTLR	SB_CLK48M_USBCTLR - @k2_lib.K2	7B8 25D3 30C6 105B3
SB_CRT_TVOUT_MUX_L	SB_CRT_TVOUT_MUX_L - @k2_lib.K2	25D2 91A7
SB_GPIO10_CL1	SB_GPIO10_CL1 - @k2_lib.K2	25A5 25B3
SB_GPIO14_CL2	SB_GPIO14_CL2 - @k2_lib.K2	25A5 25B3
SB_GPIO18	SB_GPIO18 - @k2_lib.K2	25C5
SB_GPIO30	SB_GPIO30 - @k2_lib.K2	13C3 24C8
SB_GPIO36	SB_GPIO36 - @k2_lib.K2	25D3
SB_GPIO40	SB_GPIO40 - @k2_lib.K2	13C3 24C8
SB_INTVRMEN	SB_INTVRMEN - @k2_lib.K2	23D6
SB_LAN100_SLP	SB_LAN100_SLP - @k2_lib.K2	23C6
SB_RCIN_L	SB_RCIN_L - @k2_lib.K2	23C4
SB_RTC_RST_L	SB_RTC_RST_L - @k2_lib.K2	7B3 7B8 23D8 28D5
SB_RTC_X1	SB_RTC_X1 - @k2_lib.K2	23D8 28C8
SB_RTC_X1_R	SB_RTC_X1_R - @k2_lib.K2	28C7
SB_RTC_X2	SB_RTC_X2 - @k2_lib.K2	23D8 28C8
SB_SATALED_L	SB_SATALED_L - @k2_lib.K2	45C2
	SMC_EXCARD_OC_L - @k2_lib.K2	45C3 49B8 50B2
	TP_SB_SATALED_L - @k2_lib.K2	23B6 45C3
	SMC_EXCARD_OC_L - @k2_lib.K2	45C3 49B8 50B2
SB_SATALED_R_L	SB_SATALED_R_L - @k2_lib.K2	45C2
SB_SATA_CLKREQ_L	SB_SATA_CLKREQ_L - @k2_lib.K2	25C5 29B3 30D2
SB_SCLOCK	SB_SCLOCK - @k2_lib.K2	25C5
SB_SDATAOUT<0>	SB_SDATAOUT<0> - @k2_lib.K2	25C5
SB_SDATAOUT<1>	SB_SDATAOUT<1> - @k2_lib.K2	25C5
SB_SLOAD	SB_SLOAD - @k2_lib.K2	25C5 98C7
SB_SM_INTRUDER_L	SB_SM_INTRUDER_L - @k2_lib.K2	23D8 28D5
SB_SPKR	SB_SPKR - @k2_lib.K2	25B5
SDF3400_1	SDF3400_1 - @k2_lib.K2	34A5
SDF4721_1	SDF4721_1 - @k2_lib.K2	47D2
SENSE_12V_S0_N	SENSE_12V_S0_N - @k2_lib.K2	53B3 53B4
SENSE_12V_S0_P	SENSE_12V_S0_P - @k2_lib.K2	53B3 53B4
SENSE_12V_S5_N	SENSE_12V_S5_N - @k2_lib.K2	53B3 53C4
SENSE_12V_S5_P	SENSE_12V_S5_P - @k2_lib.K2	53B3 53B4
SMBUS_SMC_0_S0_SCL	SMBUS_SMC_0_S0_SCL - @k2_lib.K2	52D5 106B3
	=SMB_LCD_TEMP_SCL - @k2_lib.K2	52C3 55C6
	=SMB_AMB_TEMP_SCL - @k2_lib.K2	52D3 55C8
	=SMB_GPU_THRM_SCL - @k2_lib.K2	52D3 85C7
	SMB_0_S0_CLK - @k2_lib.K2	49B8 52D6
	=SMB_LCD_TEMP_SCL - @k2_lib.K2	52C3 55C6
	=SMB_GPU_THRM_SCL - @k2_lib.K2	52D3 85C7
	=SMB_AMB_TEMP_SCL - @k2_lib.K2	52D3 55C8
SMBUS_SMC_0_S0_SDA	SMBUS_SMC_0_S0_SDA - @k2_lib.K2	52D5 106B3
	=SMB_LCD_TEMP_SDA - @k2_lib.K2	52C3 55C6
	=SMB_AMB_TEMP_SDA - @k2_lib.K2	52C3 55C8
	=SMB_GPU_THRM_SDA - @k2_lib.K2	52D3 85C7
	SMB_0_S0_DATA - @k2_lib.K2	49B5 52D6
	=SMB_LCD_TEMP_SDA - @k2_lib.K2	52C3 55C6
	=SMB_GPU_THRM_SDA - @k2_lib.K2	52D3 85C7
	=SMB_AMB_TEMP_SDA - @k2_lib.K2	52C3 55C8
SMBUS_SMC_A_S3_SCL	SMBUS_SMC_A_S3_SCL - @k2_lib.K2	106B3
SMBUS_SMC_A_S3_SDA	SMBUS_SMC_A_S3_SDA - @k2_lib.K2	106B3
SMBUS_SMC_A_S5_SCL	SMBUS_SMC_A_S5_SCL - @k2_lib.K2	52D2
	SMB_A_S3_CLK - @k2_lib.K2	49A5 52D3
SMBUS_SMC_A_S5_SDA	SMBUS_SMC_A_S5_SDA - @k2_lib.K2	52D2
	SMB_A_S3_DATA - @k2_lib.K2	49A5 52D3
SMBUS_SMC_BSA_SCL	SMBUS_SMC_BSA_SCL - @k2_lib.K2	52C2 106B3
	SMB_BSA_CLK - @k2_lib.K2	49A5 52C3
SMBUS_SMC_BSA_SDA	SMBUS_SMC_BSA_SDA - @k2_lib.K2	52C2 106B3
	SMB_BSA_DATA - @k2_lib.K2	49A5 52C3
SMBUS_SMC_B_S0_SCL	SMBUS_SMC_B_S0_SCL - @k2_lib.K2	52C5 106B3
	=SMBUS_MINI_SCL - @k2_lib.K2	34B3 52B3
	=SMB_REMOTE_TEMP_SCL - @k2_lib.K2	52B3 55B2
	=SMB_CPU_THRM_SCL - @k2_lib.K2	52C3 55C4
	SMB_B_S0_CLK - @k2_lib.K2	49A5 52C5
	=SMB_REMOTE_TEMP_SCL - @k2_lib.K2	52B3 55B2
	=SMB_CPU_THRM_SCL - @k2_lib.K2	52C3 55C4
	=SMBUS_MINI_SCL - @k2_lib.K2	34B3 52B3
SMBUS_SMC_B_S0_SDA	SMBUS_SMC_B_S0_SDA - @k2_lib.K2	52B5 106B3
	=SMBUS_MINI_SDA - @k2_lib.K2	34B3 52B3
	=SMB_REMOTE_TEMP_SDA - @k2_lib.K2	52B3 55B2
	=SMB_CPU_THRM_SDA - @k2_lib.K2	52B3 55C4
	SMB_B_S0_DATA - @k2_lib.K2	49A5 52B5
	=SMB_REMOTE_TEMP_SDA - @k2_lib.K2	52B3 55B2
	=SMB_CPU_THRM_SDA - @k2_lib.K2	52B3 55C4
	=SMBUS_MINI_SDA - @k2_lib.K2	34B3 52B3
SMBUS_SMC_MGMT_SCL	SMBUS_SMC_MGMT_SCL - @k2_lib.K2	52B2 106B3
	SMB_MGMT_CLK - @k2_lib.K2	49C5 52B3
SMBUS_SMC_MGMT_SDA	SMBUS_SMC_MGMT_SDA - @k2_lib.K2	52B2 106B3
	SMB_MGMT_DATA - @k2_lib.K2	49C8 52B3
SMB_CLK	SMB_CLK - @k2_lib.K2	25D5 52D8 103A3
	=SMBUS_CK505_SCL - @k2_lib.K2	29B5 52D6
	SMBUS_SB_SCL - @k2_lib.K2	52D7
	=I2C_DIMMA_SCL - @k2_lib.K2	31A6 52D6
	=I2C_DIMMB_SCL - @k2_lib.K2	32A6 52C6
	SMBUS_SB_SCL - @k2_lib.K2	52D7
	=SMBUS_CK505_SCL - @k2_lib.K2	29B5 52D6
	=I2C_DIMMB_SCL - @k2_lib.K2	32A6 52C6
	=I2C_DIMMA_SCL - @k2_lib.K2	31A6 52D6
SMB_DATA	SMB_DATA - @k2_lib.K2	25D5 52D8 103A3

	=SMBUS_CK505_SDA - @k2_lib.K2	29B5 52D6
	SMBUS_SB_SDA - @k2_lib.K2	52D7
	=I2C_DIMMA_SDA - @k2_lib.K2	31A6 52D6
	=I2C_DIMMB_SDA - @k2_lib.K2	32A6 52C6
	SMBUS_SB_SDA - @k2_lib.K2	52D7
	=SMBUS_CK505_SDA - @k2_lib.K2	29B5 52D6
	=I2C_DIMMB_SDA - @k2_lib.K2	32A6 52C6
	=I2C_DIMMA_SDA - @k2_lib.K2	31A6 52D6
SMB_ME_CLK	SMB_ME_CLK - @k2_lib.K2	25D5 52A8 103A3
	SMBUS_SB_ME_SCL - @k2_lib.K2	52A7
SMB_ME_DATA	SMB_ME_DATA - @k2_lib.K2	25D5 52A8 103A3
	SMBUS_SB_ME_SDA - @k2_lib.K2	52A7
SMC_12V_S0_ISENSE	SMC_12V_S0_ISENSE - @k2_lib.K2	50B3 53B1
	SMC_DCIN_ISENSE - @k2_lib.K2	49C5 50B5
SMC_12V_S0_ISENSE_R	SMC_12V_S0_ISENSE_R - @k2_lib.K2	53B2
SMC_12V_S0_VSENSE	SMC_12V_S0_VSENSE - @k2_lib.K2	50B3 53B2
	SMC_PBUS_VSENSE - @k2_lib.K2	49C5 50B5
SMC_12V_S5_ISENSE	SMC_12V_S5_ISENSE - @k2_lib.K2	50B3 53B1
	SMC_BATT_ISENSE - @k2_lib.K2	49C5 50B5
SMC_12V_S5_ISENSE_R	SMC_12V_S5_ISENSE_R - @k2_lib.K2	53B2
SMC_12V_S5_VSENSE	SMC_12V_S5_VSENSE - @k2_lib.K2	50A3 53B3
	SMC_NB_1V25_ISENSE - @k2_lib.K2	49C5 50A5
SMC_ADAPTER_EN	SMC_ADAPTER_EN - @k2_lib.K2	49D5 50B5
	TP_SMC_ADAPTER_EN - @k2_lib.K2	50B3
SMC_BC_ACOK	SMC_BC_ACOK - @k2_lib.K2	49C5 50B2
SMC_BS_ALRT_L	SMC_BS_ALRT_L - @k2_lib.K2	49C5 50B2
SMC_CASE_OPEN	SMC_CASE_OPEN - @k2_lib.K2	49B5 50A2
SMC_CPU_ISENSE	SMC_CPU_ISENSE - @k2_lib.K2	49C5 53C6
SMC_CPU_VSENSE	SMC_CPU_VSENSE - @k2_lib.K2	49C5 53D6
SMC_EXCARD_CP	SMC_EXCARD_CP - @k2_lib.K2	49B8 50A2
SMC_EXCARD_PWR_EN	SMC_EXCARD_PWR_EN - @k2_lib.K2	49B8 50B5
	TP_SMC_EXCARD_PWR_EN - @k2_lib.K2	50B3
SMC_EXTAL	SMC_EXTAL - @k2_lib.K2	49C3 50C8
SMC_FAN_0_CTL	SMC_FAN_0_CTL - @k2_lib.K2	49A8 56D8
SMC_FAN_0_TACH	SMC_FAN_0_TACH - @k2_lib.K2	49A8 56C8
SMC_FAN_1_CTL	SMC_FAN_1_CTL - @k2_lib.K2	49A8 56B8
SMC_FAN_1_TACH	SMC_FAN_1_TACH - @k2_lib.K2	49A8 56A8
SMC_FAN_2_CTL	SMC_FAN_2_CTL - @k2_lib.K2	49A8 57D8
SMC_FAN_2_TACH	SMC_FAN_2_TACH - @k2_lib.K2	49A8 57C8
SMC_FAN_3_CTL	SMC_FAN_3_CTL - @k2_lib.K2	49A8 50C5
	TP_SMC_FAN_3_CTL - @k2_lib.K2	50C3
SMC_FAN_3_TACH	SMC_FAN_3_TACH - @k2_lib.K2	49A8 50C5
	TP_SMC_FAN_3_TACH - @k2_lib.K2	50C3
SMC_FWE	SMC_FWE - @k2_lib.K2	49A5 50B2
SMC_GFX_OVERTEMP_L	SMC_GFX_OVERTEMP_L - @k2_lib.K2	49A8 85C8
SMC_GFX_THROTTLE_L	SMC_GFX_THROTTLE_L - @k2_lib.K2	49C8 85B7
SMC_GPU_ISENSE	SMC_GPU_ISENSE - @k2_lib.K2	49C5 53C3
SMC_GPU_VSENSE	SMC_GPU_VSENSE - @k2_lib.K2	49C5 53D3
SMC_KBC_MDE	SMC_KBC_MDE - @k2_lib.K2	49C2
SMC_LID	SMC_LID - @k2_lib.K2	49B5 50B2
SMC_LRESET_L	SMC_LRESET_L - @k2_lib.K2	7C6 28D1 49C8
SMC_MANUAL_RST_L	SMC_MANUAL_RST_L - @k2_lib.K2	50D7
SMC_MD1	SMC_MD1 - @k2_lib.K2	7D4 49C1 51B6
SMC_NMI	SMC_NMI - @k2_lib.K2	7C4 49C1 51B4
SMC_ODD_DETECT	SMC_ODD_DETECT - @k2_lib.K2	44B3 49B8
SMC_ONOFF_L	SMC_ONOFF_L - @k2_lib.K2	49C5 50B2 50C5
SMC_P14	SMC_P14 - @k2_lib.K2	49D8 50D5
	TP_SMC_P14 - @k2_lib.K2	50D3
SMC_P20	SMC_P20 - @k2_lib.K2	49C8 50D5
	TP_SMC_P20 - @k2_lib.K2	50D3
SMC_P21	SMC_P21 - @k2_lib.K2	49C8 50C5
	TP_SMC_P21 - @k2_lib.K2	50C3
SMC_P22	SMC_P22 - @k2_lib.K2	49C8 50C5
	TP_SMC_P22 - @k2_lib.K2	50C3
SMC_P23	SMC_P23 - @k2_lib.K2	49C8 50C5
	TP_SMC_P23 - @k2_lib.K2	50C3
SMC_P26	SMC_P26 - @k2_lib.K2	49C8 50C5
	TP_SMC_P26 - @k2_lib.K2	50C3
SMC_P27	SMC_P27 - @k2_lib.K2	49C8 50C5
	TP_SMC_P27 - @k2_lib.K2	50C3
SMC_P43	SMC_P43 - @k2_lib.K2	49C8 50C5
	TP_SMC_P43 - @k2_lib.K2	50C3
SMC_P44	SMC_P44 - @k2_lib.K2	49C8 50C5
	TP_SMC_P44 - @k2_lib.K2	50C3
SMC_P45	SMC_P45 - @k2_lib.K2	49C8 50C5
	TP_SMC_P45 - @k2_lib.K2	50C3
SMC_P46	SMC_P46 - @k2_lib.K2	49B8 50B5
	TP_SMC_P46 - @k2_lib.K2	50B3
SMC_P62	SMC_P62 - @k2_lib.K2	49D5 50C5
	TP_SMC_P62 - @k2_lib.K2	50C3
SMC_P63	SMC_P63 - @k2_lib.K2	49D5 50C5
	TP_SMC_P63 - @k2_lib.K2	50C3
SMC_P64	SMC_P64 - @k2_lib.K2	49D5 50C5
	TP_SMC_P64 - @k2_lib.K2	50C3
SMC_P67	SMC_P67 - @k2_lib.K2	49C5 50B2
SMC_P81	SMC_P81 - @k2_lib.K2	49C5 50C5
	TP_SMC_P81 - @k2_lib.K2	50C3
SMC_PA0	SMC_PA0 - @k2_lib.K2	49B8 50B2
SMC_PA1	SMC_PA1 - @k2_lib.K2	49B8 50B2
SMC_PB0	SMC_PB0 - @k2_lib.K2	49B8 50B2
SMC_PF0	SMC_PF0 - @k2_lib.K2	49B5 50C5
	TP_SMC_PF0 - @k2_lib.K2	50C3
SMC_PF1	SMC_PF1 - @k2_lib.K2	49B5 50C5
	TP_SMC_PF1 - @k2_lib.K2	50C3
SMC_PF3	SMC_PF3 - @k2_lib.K2	49B5 50B2
SMC_PG0	SMC_PG0 - @k2_lib.K2	49B5 50B2
SMC_PH4	SMC_PH4 - @k2_lib.K2	49A5 50B2
SMC_PM_G2_EN	SMC_PM_G2_EN - @k2_lib.K2	49D5 50C5
	TP_SMC_PM_G2_EN - @k2_lib.K2	50C3
SMC_PROCHOT	SMC_PROCHOT - @k2_lib.K2	49A5 50C1
SMC_PROCHOT_3_3_L	SMC_PROCHOT_3_3_L - @k2_lib.K2	49C5 50D1
SMC_RESET_L	SMC_RESET_L - @k2_lib.K2	7C4 7C6 49C3 50D6 51B4
SMC_RSTGATE_L	SMC_RSTGATE_L - @k2_lib.K2	49D8 50B5
	TP_SMC_RSTGATE_L - @k2_lib.K2	50B3
SMC_RUNTIME_SCI_L	SMC_RUNTIME_SCI_L - @k2_lib.K2	25C8 49B8
SMC_RX_L	SMC_RX_L - @k2_lib.K2	7C4 46D5 49B8 49C5 50B2 51B4
SMC_SUS_CLK	SMC_SUS_CLK - @k2_lib.K2	49C5 50C3
	SUS_CLK_SB - @k2_lib.K2	25D3 50C2
SMC_SYS_KBDLED	SMC_SYS_KBDLED - @k2_lib.K2	49B8 50B5
	TP_SMC_SYS_KBDLED - @k2_lib.K2	50B3
SMC_SYS_LED	SMC_SYS_LED - @k2_lib.K2	49C8 50B5
	TP_SMC_SYS_LED - @k2_lib.K2	50B3
SMC_TCK	SMC_TCK - @k2_lib.K2	7D4 49B5 50B2 51B4
SMC_TDI	SMC_TDI - @k2_lib.K2	7D4 49B5 50B2 51B4
SMC_TDO	SMC_TDO - @k2_lib.K2	7D4 49B5 50B2 51B6
SMC_THRMTRIP	SMC_THRMTRIP - @k2_lib.K2	49A5 50C1
SMC_TMS	SMC_TMS - @k2_lib.K2	7D4 49B5 50B2 51B6
SMC_TRST_L	SMC_TRST_L - @k2_lib.K2	7D4 49C1 51B6
SMC_TX_L	SMC_TX_L - @k2_lib.K2	7D4 46D5 49B8 49C5 50B2 51B6
SMC_VCL	SMC_VCL - @k2_lib.K2	49D2
SMC_WAKE_SCI_L	SMC_WAKE_SCI_L - @k2_lib.K2	13C3 25C8 49C5
SMC_XTAL	SMC_XTAL - @k2_lib.K2	49C3 50C8
SMS_ONOFF_L	SMS_ONOFF_L - @k2_lib.K2	49A5 50B5
	TP_SMS_ONOFF_L - @k2_lib.K2	50B3
SMS_X_AXIS	SMS_X_AXIS - @k2_lib.K2	49A8 50D5 108D1
	NC_SMS_X_AXIS - @k2_lib.K2	50D3
SMS_Y_AXIS	SMS_Y_AXIS - @k2_lib.K2	49A8 50D5 108D1
	NC_SMS_Y_AXIS - @k2_lib.K2	50D3
SMS_Z_AXIS	SMS_Z_AXIS - @k2_lib.K2	49A8 50D5 108D1
	NC_SMS_Z_AXIS - @k2_lib.K2	50D3
SPI_A_SCLK_R	SPI_A_SCLK_R - @k2_lib.K2	103A3
SPI_A_SI_R	SPI_A_SI_R - @k2_lib.K2	61B4 103A3
SPI_A_SO_R	SPI_A_SO_R - @k2_lib.K2	7B3 61B4 103A3
SPI_B_SCLK_R	SPI_B_SCLK_R - @k2_lib.K2	103A3
SPI_B_SI_R	SPI_B_SI_R - @k2_lib.K2	103A3
SPI_B_SO	SPI_B_SO - @k2_lib.K2	103A3
SPI_B_SO_R	SPI_B_SO_R - @k2_lib.K2	103A3
SPI_CE_L<0>	SPI_CE_L<0> - @k2_lib.K2	7B3 61B6 103A3
SPI_CE_L<1>	SPI_CE_L<1> - @k2_lib.K2	103A3
SPI_CE_R_L<0>	SPI_CE_R_L<0> - @k2_lib.K2	24C5 61B7 103A3
SPI_CE_R_L<1>	SPI_CE_R_L<1> - @k2_lib.K2	103A3
SPI_HOLD_L	SPI_HOLD_L - @k2_lib.K2	61B5
SPI_SCLK	SPI_SCLK - @k2_lib.K2	7B3 61B6 103A3
SPI_SCLK_R	SPI_SCLK_R - @k2_lib.K2	7A8 24C5 61B7 103A3
SPI_SI	SPI_SI - @k2_lib.K2	103A3
SPI_SI_R	SPI_SI_R - @k2_lib.K2	24C5 61B3 103A3
SPI_SO	SPI_SO - @k2_lib.K2	7A8 24C5 61B3 103A3
SPI_WP_L	SPI_WP_L - @k2_lib.K2	61B5
SYS_ONEWIRE	SYS_ONEWIRE - @k2_lib.K2	49B8 50B2
TMDS_CLK_N	TMDS_CLK_N - @k2_lib.K2	85A7 94C8 108D3
TMDS_CLK_P	TMDS_CLK_P - @k2_lib.K2	85A7 94B8 108D3
TMDS_CONN_CLKN	TMDS_CONN_CLKN - @k2_lib.K2	94C4 94C7 108D3
TMDS_CONN_CLKP	TMDS_CONN_CLKP - @k2_lib.K2	94B7 94C4 108D3
TMDS_CONN_DN<0>	TMDS_CONN_DN<0> - @k2_lib.K2	94C4 94D6
TMDS_CONN_DN<3..0>	TMDS_CONN_DN<3..0> - @k2_lib.K2	108D3
TMDS_CONN_DN<1>	TMDS_CONN_DN<1> - @k2_lib.K2	94C4 94D6
TMDS_CONN_DN<2>	TMDS_CONN_DN<2> - @k2_lib.K2	94C6 94D4
TMDS_CONN_DP<0>	TMDS_CONN_DP<0> - @k2_lib.K2	94C4 94D6
TMDS_CONN_DP<3..0>	TMDS_CONN_DP<3..0> - @k2_lib.K2	108D3
TMDS_CONN_DP<1>	TMDS_CONN_DP<1> - @k2_lib.K2	94C4 94D6
TMDS_CONN_DP<2>	TMDS_CONN_DP<2> - @k2_lib.K2	94C6 94D4
TMDS_DATA_N<0>	TMDS_DATA_N<0> - @k2_lib.K2	85A7 94D8
TMDS_DATA_N<3..0>	TMDS_DATA_N<3..0> - @k2_lib.K2	108D3
TMDS_DATA_N<1>	TMDS_DATA_N<1> - @k2_lib.K2	85A7 94D8
TMDS_DATA_N<2>	TMDS_DATA_N<2> - @k2_lib.K2	85A7 94C8
TMDS_DATA_P<0>	TMDS_DATA_P<0> - @k2_lib.K2	85A7 94D8
TMDS_DATA_P<3..0>	TMDS_DATA_P<3..0> - @k2_lib.K2	108D3
TMDS_DATA_P<1>	TMDS_DATA_P<1> - @k2_lib.K2	85A7 94C8
TMDS_DATA_P<2>	TMDS_DATA_P<2> - @k2_lib.K2	85A7 94C8
TP_CK505_PGMODE	TP_CK505_PGMODE - @k2_lib.K2	7D2 29B5
TP_CPU_RSVD0	TP_CPU_RSVD0 - @k2_lib.K2	10B8
TP_CPU_RSVD1	TP_CPU_RSVD1 - @k2_lib.K2	10B8
TP_CPU_RSVD2	TP_CPU_RSVD2 - @k2_lib.K2	10B8
TP_CPU_RSVD3	TP_CPU_RSVD3 - @k2_lib.K2	10B8
TP_CPU_RSVD4	TP_CPU_RSVD4 - @k2_lib.K2	10B8
TP_CPU_RSVD5	TP_CPU_RSVD5 - @k2_lib.K2	10B8
TP_CPU_RSVD6	TP_CPU_RSVD6 - @k2_lib.K2	10B8
TP_CPU_RSVD7	TP_CPU_RSVD7 - @k2_lib.K2	10B8
TP_CPU_RSVD8	TP_CPU_RSVD8 - @k2_lib.K2	10B8
TP_CPU_RSVD9	TP_CPU_RSVD9 - @k2_lib.K2	10B8
TP_CPU_TEST3	TP_CPU_TEST3 - @k2_lib.K2	10B4
TP_CPU_TEST5	TP_CPU_TEST5 - @k2_lib.K2	10B4
TP_CPU_TEST6	TP_CPU_TEST6 - @k2_lib.K2	10B4
TP_ENET_GLAN_CLK	TP_ENET_GLAN_CLK - @k2_lib.K2	23C6
TP_FW_AVREG	TP_FW_AVREG - @k2_lib.K2	40B6
TP_FW_CE	TP_FW_CE - @k2_lib.K2	7B3 40B6
TP_FW_FW620_L	TP_FW_FW620_L - @k2_lib.K2	40B6
TP_FW_JASI_EN	TP_FW_JASI_EN - @k2_lib.K2	40B6
TP_FW_MODE_A	TP_FW_MODE_A - @k2_lib.K2	40B6
TP_FW_NAND_TREE	TP_FW_NAND_TREE - @k2_lib.K2	7C3 40B6
TP_FW_SCIFCLK	TP_FW_SCIFCLK - @k2_lib.K2	40B3
TP_FW_SCIFDAIN	TP_FW_SCIFDAIN - @k2_lib.K2	40B3
TP_FW_SCIFDOUT	TP_FW_SCIFDOUT - @k2_lib.K2	40B3
TP_FW_SCIFMC	TP_FW_SCIFMC - @k2_lib.K2	40B3
TP_FW_SDA	TP_FW_SDA - @k2_lib.K2	40B3
TP_FW_SE	TP_FW_SE - @k2_lib.K2	7C3 40B6
TP_FW_SM	TP_FW_SM - @k2_lib.K2	7C3 40B6
TP_FW_TCK	TP_FW_TCK - @k2_lib.K2	7C3 40C3
TP_FW_TDI	TP_FW_TDI - @k2_lib.K2	7C3 40C3
TP_FW_TDO	TP_FW_TDO - @k2_lib.K2	7C3 40C3
TP_FW_TMS	TP_FW_TMS - @k2_lib.K2	7C3 40C3
TP_FW_VAUX_DISABLE	TP_FW_VAUX_DISABLE - @k2_lib.K2	40C3
TP_FW_VBUF	TP_FW_VBUF - @k2_lib.K2	40B6
TP_GPU_DDC_B_CLK	TP_GPU_DDC_B_CLK - @k2_lib.K2	85A4
TP_GPU_DDC_B_DATA	TP_GPU_DDC_B_DATA - @k2_lib.K2	85A4
TP_HDA_DOCK_RST_L	TP_HDA_DOCK_RST_L - @k2_lib.K2	23B6
TP_HDA_SDIN1	TP_HDA_SDIN1 - @k2_lib.K2	23C8
TP_HDA_SDIN2	TP_HDA_SDIN2 - @k2_lib.K2	23C8
TP_HDA_SDIN3	TP_HDA_SDIN3 - @k2_lib.K2	23C8
TP_LAN_D2R<0>	TP_LAN_D2R<0> - @k2_lib.K2	23C6
TP_LAN_D2R<1>	TP_LAN_D2R<1> - @k2_lib.K2	23C6
TP_LAN_D2R<2>	TP_LAN_D2R<2> - @k2_lib.K2	7D2 23C6 28C4
TP_LAN_R2D<0>	TP_LAN_R2D<0> - @k2_lib.K2	23C6
TP_LAN_R2D<1>	TP_LAN_R2D<1> - @k2_lib.K2	23C6
TP_LAN_R2D<2>	TP_LAN_R2D<2> - @k2_lib.K2	23C6
TP_LAN_RSTSYNC	TP_LAN_RSTSYNC - @k2_lib.K2	23C6
TP_LPC_DRQ0_L	TP_LPC_DRQ0_L - @k2_lib.K2	23D4
TP_LVDS_A_DATAN3	TP_LVDS_A_DATAN3 - @k2_lib.K2	16C6
TP_LVDS_A_DATAP3	TP_LVDS_A_DATAP3 - @k2_lib.K2	16C6
TP_LVDS_B_DATAN3	TP_LVDS_B_DATAN3 - @k2_lib.K2	16C6
TP_LVDS_B_DATAP3	TP_LVDS_B_DATAP3 - @k2_lib.K2	16C6
TP_LVDS_VBG	TP_LVDS_VBG - @k2_lib.K2	15D5
TP_MEM_A_A<15>	TP_MEM_A_A<15> - @k2_lib.K2	31C3
TP_MEM_A_RCVEN_L	TP_MEM_A_RCVEN_L - @k2_lib.K2	17B5
TP_MEM_B_A<15>	TP_MEM_B_A<15> - @k2_lib.K2	32C3
TP_MEM_B_RCVEN_L	TP_MEM_B_RCVEN_L - @k2_lib.K2	17B2
TP_MEM_CLKN2	TP_MEM_CLKN2 - @k2_lib.K2	16C6
TP_MEM_CLKN5	TP_MEM_CLKN5 - @k2_lib.K2	16C6
TP_MEM_CLKP2	TP_MEM_CLKP2 - @k2_lib.K2	16C6
TP_MEM_CLKP5	TP_MEM_CLKP5 - @k2_lib.K2	16C6
TP_NB_CFG<10>	TP_NB_CFG<10> - @k2_lib.K2	16B6
TP_NB_CFG<11>	TP_NB_CFG<11> - @k2_lib.K2	16B6
TP_NB_CFG<12>	TP_NB_CFG<12> - @k2_lib.K2	7C3 16B6
TP_NB_CFG<13>	TP_NB_CFG<13> - @k2_lib.K2	7C3 16B6
TP_NB_CFG<14>	TP_NB_CFG<14> - @k2_lib.K2	16B6
TP_NB_CFG<15>	TP_NB_CFG<15> - @k2_lib.K2	16B6
TP_NB_CFG<17>	TP_NB_CFG<17> - @k2_lib.K2	16B6
TP_NB_CFG<18>	TP_NB_CFG<18> - @k2_lib.K2	7C3 16B6
TP_NB_NC<1>	TP_NB_NC<1> - @k2_lib.K2	7D2 16A6
TP_NB_NC<2>	TP_NB_NC<2> - @k2_lib.K2	7D2 16A6
TP_NB_NC<3>	TP_NB_NC<3> - @k2_lib.K2	7D2 16A6
TP_NB_NC<4>	TP_NB_NC<4> - @k2_lib.K2	7D2 16A6
TP_NB_NC<5>	TP_NB_NC<5> - @k2_lib.K2	7D2 16A6
TP_NB_NC<6>	TP_NB_NC<6> - @k2_lib.K2	16A6
TP_NB_NC<7>	TP_NB_NC<7> - @k2_lib.K2	16A6
TP_NB_NC<8>	TP_NB_NC<8> - @k2_lib.K2	16A6
TP_NB_NC<9>	TP_NB_NC<9> - @k2_lib.K2	16A6
TP_NB_NC<10>	TP_NB_NC<10> - @k2_lib.K2	16A6
TP_NB_NC<11>	TP_NB_NC<11> - @k2_lib.K2	16A6
TP_NB_NC<12>	TP_NB_NC<12> - @k2_lib.K2	16A6
TP_NB_NC<13>	TP_NB_NC<13> - @k2_lib.K2	16A6
TP_NB_NC<14>	TP_NB_NC<14> - @k2_lib.K2	16A6
TP_NB_NC<15>	TP_NB_NC<15> - @k2_lib.K2	16A6
TP_NB_NC<16>	TP_NB_NC<16> - @k2_lib.K2	16A6
TP_NB_RSVD<1>	TP_NB_RSVD<1> - @k2_lib.K2	16D6
TP_NB_RSVD<2>	TP_NB_RSVD<2> - @k2_lib.K2	16D6
TP_NB_RSVD<3>	TP_NB_RSVD<3> - @k2_lib.K2	16D6
TP_NB_RSVD<4>	TP_NB_RSVD<4> - @k2_lib.K2	16D6
TP_NB_RSVD<5>	TP_NB_RSVD<5> - @k2_lib.K2	16D6
TP_NB_RSVD<6>	TP_NB_RSVD<6> - @k2_lib.K2	16D6
TP_NB_RSVD<7>	TP_NB_RSVD<7> - @k2_lib.K2	16D6
TP_NB_RSVD<8>	TP_NB_RSVD<8> - @k2_lib.K2	16D6
TP_NB_RSVD<9>	TP_NB_RSVD<9> - @k2_lib.K2	16D6
TP_NB_RSVD<10>	TP_NB_RSVD<10> - @k2_lib.K2	7B3 16D6
TP_NB_RSVD<11>	TP_NB_RSVD<11> - @k2_lib.K2	7B3 16D6
TP_NB_RSVD<12>	TP_NB_RSVD<12> - @k2_lib.K2	7B3 16D6
TP_NB_RSVD<13>	TP_NB_RSVD<13> - @k2_lib.K2	7B3 16D6
TP_NB_RSVD<14>	TP_NB_RSVD<14> - @k2_lib.K2	16D6
TP_NB_RSVD<20>	TP_NB_RSVD<20> - @k2_lib.K2	16D6
TP_NB_RSVD<21>	TP_NB_RSVD<21> - @k2_lib.K2	16D6
TP_NB_RSVD<22>	TP_NB_RSVD<22> - @k2_lib.K2	16C6
TP_NB_RSVD<23>	TP_NB_RSVD<23> - @k2_lib.K2	16C6
TP_NB_RSVD<24>	TP_NB_RSVD<24> - @k2_lib.K2	16C6
TP_NB_RSVD<25>	TP_NB_RSVD<25> - @k2_lib.K2	16C6
TP_NB_RSVD<26>	TP_NB_RSVD<26> - @k2_lib.K2	16C6
TP_NB_RSVD<27>	TP_NB_RSVD<27> - @k2_lib.K2	16C6
TP_NB_RSVD<34>	TP_NB_RSVD<34> - @k2_lib.K2	16C6
TP_NB_RSVD<35>	TP_NB_RSVD<35> - @k2_lib.K2	16C6
TP_NB_RSVD<36>	TP_NB_RSVD<36> - @k2_lib.K2	16C6
TP_NB_RSVD<41>	TP_NB_RSVD<41> - @k2_lib.K2	16C6
TP_NB_RSVD<42>	TP_NB_RSVD<42> - @k2_lib.K2	16C6
TP_NB_RSVD<43>	TP_NB_RSVD<43> - @k2_lib.K2	16C6
TP_NB_RSVD<44>	TP_NB_RSVD<44> - @k2_lib.K2	16C6
TP_NB_RSVD<45>	TP_NB_RSVD<45> - @k2_lib.K2	16C6
TP_PCIE_A_D2R_N	TP_PCIE_A_D2R_N - @k2_lib.K2	24D5
TP_PCIE_A_D2R_P	TP_PCIE_A_D2R_P - @k2_lib.K2	24D5
TP_PCIE_A_R2D_C_N	TP_PCIE_A_R2D_C_N - @k2_lib.K2	24D5
TP_PCIE_A_R2D_C_P	TP_PCIE_A_R2D_C_P - @k2_lib.K2	24D5
TP_PCIE_B_D2R_N	TP_PCIE_B_D2R_N - @k2_lib.K2	24D5
TP_PCIE_B_D2R_P	TP_PCIE_B_D2R_P - @k2_lib.K2	24D5
TP_PCIE_B_R2D_C_N	TP_PCIE_B_R2D_C_N - @k2_lib.K2	24D5
TP_PCIE_B_R2D_C_P	TP_PCIE_B_R2D_C_P - @k2_lib.K2	24D5
TP_PCIE_EXCARD_D2R_N	TP_PCIE_EXCARD_D2R_N - @k2_lib.K2	24D5
TP_PCIE_EXCARD_D2R_P	TP_PCIE_EXCARD_D2R_P - @k2_lib.K2	24D5
TP_PCIE_EXCARD_R2D_C_N	TP_PCIE_EXCARD_R2D_C_N - @k2_lib.K2	24D5
TP_PCIE_EXCARD_R2D_C_P	TP_PCIE_EXCARD_R2D_C_P - @k2_lib.K2	24D5
TP_PCI_PME_L	TP_PCI_PME_L - @k2_lib.K2	24A6
TP_PM_SLP_M_L	TP_PM_SLP_M_L - @k2_lib.K2	25C3
TP_PM_SLP_S4_L	TP_PM_SLP_S4_L - @k2_lib.K2	25D3
TP_PP5VREG_PLLIN	TP_PP5VREG_PLLIN - @k2_lib.K2	76B5
TP_SB_GPIO51	TP_SB_GPIO51 - @k2_lib.K2	24B6
TP_SB_GPIO53	TP_SB_GPIO53 - @k2_lib.K2	24B6
TP_SB_GPIO55	TP_SB_GPIO55 - @k2_lib.K2	24B6
TP_SB_TP3	TP_SB_TP3 - @k2_lib.K2	25B5
TP_SB_TP7	TP_SB_TP7 - @k2_lib.K2	25C5
TP_SB_TP8	TP_SB_TP8 - @k2_lib.K2	23C4
TP_SPI_CE_R_L<1>	TP_SPI_CE_R_L<1> - @k2_lib.K2	24C5
TP_VCCCL1_05_INTERNAL_REG	TP_VCCCL1_05_INTERNAL_REG - @k2_lib.K2	26A3
TP_VCCLAN1_05_INTERNAL_REG1	TP_VCCLAN1_05_INTERNAL_REG1 - @k2_lib.K2	26A6
TP_VCCLAN1_05_INTERNAL_REG2	TP_VCCLAN1_05_INTERNAL_REG2 - @k2_lib.K2	26A6
TP_VCCSUS1_05_INTERNAL_REG1	TP_VCCSUS1_05_INTERNAL_REG1 - @k2_lib.K2	26B3
TP_VCCSUS1_05_INTERNAL_REG2	TP_VCCSUS1_05_INTERNAL_REG2 - @k2_lib.K2	26B3
TP_VCCSUS1_5_INTERNAL_REG1	TP_VCCSUS1_5_INTERNAL_REG1 - @k2_lib.K2	26B3
TP_VCCSUS1_5_INTERNAL_REG2	TP_VCCSUS1_5_INTERNAL_REG2 - @k2_lib.K2	26B3
TP_XDP_HOOK2	TP_XDP_HOOK2 - @k2_lib.K2	13B6
TP_XDP_HOOK3	TP_XDP_HOOK3 - @k2_lib.K2	13B6
U5500_TCRIT1	U5500_TCRIT1 - @k2_lib.K2	55B3
U5500_TCRIT2	U5500_TCRIT2 - @k2_lib.K2	55B3
U5500_TCRIT3	U5500_TCRIT3 - @k2_lib.K2	55A3
U7550_VDDQ	U7550_VDDQ - @k2_lib.K2	75B5
USB_BT_N	USB_BT_N - @k2_lib.K2	7A8 24C2 47D3 103B3
USB_BT_P	USB_BT_P - @k2_lib.K2	7A8 24C2 47D3 103B3
USB_CAMERA_L_N	USB_CAMERA_L_N - @k2_lib.K2	47B5 108C3
USB_CAMERA_L_P	USB_CAMERA_L_P - @k2_lib.K2	47B5 108C3
USB_CAMERA_N	USB_CAMERA_N - @k2_lib.K2	7A8 24C2 47B7 103B3
USB_CAMERA_P	USB_CAMERA_P - @k2_lib.K2	7A8 24C2 47B7 103B3
USB_C_MUXED_N	USB_C_MUXED_N - @k2_lib.K2	46D3 108C3
USB_C_MUXED_P	USB_C_MUXED_P - @k2_lib.K2	46D3 108D3
USB_DEBUGPRT_EN_L	USB_DEBUGPRT_EN_L - @k2_lib.K2	46C4 49B8
USB_EXCARD_N	USB_EXCARD_N - @k2_lib.K2	24C2 47B3 103B3
	TP_USB_EXCARD_N - @k2_lib.K2	47B1
USB_EXCARD_P	USB_EXCARD_P - @k2_lib.K2	24C2 47B3 103B3
	TP_USB_EXCARD_P - @k2_lib.K2	47B1
USB_EXTA_MUXED_N	USB_EXTA_MUXED_N - @k2_lib.K2	103B3
USB_EXTA_MUXED_P	USB_EXTA_MUXED_P - @k2_lib.K2	103B3
USB_EXTA_N	USB_EXTA_N - @k2_lib.K2	24C2 46A7 103B3
USB_EXTA_OC_L	USB_EXTA_OC_L - @k2_lib.K2	13C3 24C8 46C8
USB_EXTA_P	USB_EXTA_P - @k2_lib.K2	24C2 46A7 103B3
USB_EXTB_N	USB_EXTB_N - @k2_lib.K2	24C2 46B7 103B3
USB_EXTB_OC_L	USB_EXTB_OC_L - @k2_lib.K2	13C3 24C8 46C8
USB_EXTB_P	USB_EXTB_P - @k2_lib.K2	24C2 46B7 103B3
USB_EXTC_N	USB_EXTC_N - @k2_lib.K2	24C2 46D5 103A3
USB_EXTC_OC_L	USB_EXTC_OC_L - @k2_lib.K2	24C8 46D8
USB_EXTC_P	USB_EXTC_P - @k2_lib.K2	24C2 46D5 103B3
USB_EXTD_N	USB_EXTD_N - @k2_lib.K2	24C2 46B3 103B3
	TP_USB_EXTD_N - @k2_lib.K2	46B2
USB_EXTD_OC_L	USB_EXTD_OC_L - @k2_lib.K2	13C3 24C8
USB_EXTD_P	USB_EXTD_P - @k2_lib.K2	24C2 46B3 103B3
	TP_USB_EXTD_P - @k2_lib.K2	46B2
USB_IR_L_N	USB_IR_L_N - @k2_lib.K2	47A3 47A5 108C3
USB_IR_L_P	USB_IR_L_P - @k2_lib.K2	47A3 47A5 108C3
USB_IR_N	USB_IR_N - @k2_lib.K2	7A8 24C2 47A7 103B3
USB_IR_P	USB_IR_P - @k2_lib.K2	7A8 24C2 47A7 103B3
USB_MINI_N	USB_MINI_N - @k2_lib.K2	24C2 34B3 103B3
USB_MINI_P	USB_MINI_P - @k2_lib.K2	24C2 34B3 103B3
USB_PORT0_N	USB_PORT0_N - @k2_lib.K2	46A5 108D3
USB_PORT0_P	USB_PORT0_P - @k2_lib.K2	46A5 108D3
USB_PORT1_N	USB_PORT1_N - @k2_lib.K2	46B5 108D3
USB_PORT1_P	USB_PORT1_P - @k2_lib.K2	46B5 108D3
USB_PORT2_N	USB_PORT2_N - @k2_lib.K2	46D2 108D3
USB_PORT2_P	USB_PORT2_P - @k2_lib.K2	46D2 108D3
USB_PWR_ENA_L	USB_PWR_ENA_L - @k2_lib.K2	46D8
USB_RBIAS	USB_RBIAS - @k2_lib.K2	24B3 103A3
USB_TPAD_N	USB_TPAD_N - @k2_lib.K2	24C2 47B3 103B3
	TP_USB_TPAD_N - @k2_lib.K2	47B1
USB_TPAD_P	USB_TPAD_P - @k2_lib.K2	24C2 47B3 103B3
	TP_USB_TPAD_P - @k2_lib.K2	47B1
VCCCL1_5V	VCCCL1_5V - @k2_lib.K2	26A4
VGA_BLU	VGA_BLU - @k2_lib.K2	91A4 94C5 108A3
VGA_GRN	VGA_GRN - @k2_lib.K2	91B4 94C5 108A3
VGA_HSYNC	VGA_HSYNC - @k2_lib.K2	91A2 94C5 108A3
VGA_HSYNC_R	VGA_HSYNC_R - @k2_lib.K2	91A3
VGA_RED	VGA_RED - @k2_lib.K2	91B4 94C5 108A3
VGA_VSYNC	VGA_VSYNC - @k2_lib.K2	91B2 94C5 108A3
VGA_VSYNC_R	VGA_VSYNC_R - @k2_lib.K2	91B3
VIDEO_MUX_BLU	VIDEO_MUX_BLU - @k2_lib.K2	91B7 108A3
VIDEO_MUX_GRN	VIDEO_MUX_GRN - @k2_lib.K2	91B7 108A3
VIDEO_MUX_RED	VIDEO_MUX_RED - @k2_lib.K2	91B7 108A3
VR_PWRGD_CLKEN	VR_PWRGD_CLKEN - @k2_lib.K2	7C4 25C5 28A6
VR_PWRGD_CLKEN_L	VR_PWRGD_CLKEN_L - @k2_lib.K2	28A8 71C7
WOL_EN	WOL_EN - @k2_lib.K2	25B3
WOW_EN	WOW_EN - @k2_lib.K2	13C3 24C8
XDP_BPM_L<0>	XDP_BPM_L<0> - @k2_lib.K2	10C6 13C6
XDP_BPM_L<4..0>	XDP_BPM_L<4..0> - @k2_lib.K2	100A3
XDP_BPM_L<1>	XDP_BPM_L<1> - @k2_lib.K2	10C6 13C6
XDP_BPM_L<2>	XDP_BPM_L<2> - @k2_lib.K2	10C6 13C6
XDP_BPM_L<3>	XDP_BPM_L<3> - @k2_lib.K2	10C6 13C6
XDP_BPM_L<4>	XDP_BPM_L<4> - @k2_lib.K2	10C6 13C6
XDP_BPM_L<5>	XDP_BPM_L<5> - @k2_lib.K2	10C5 13C6 100A3
XDP_CPURST_L	XDP_CPURST_L - @k2_lib.K2	13B4
XDP_DBRESET_L	XDP_DBRESET_L - @k2_lib.K2	10C6 13B3 28A5
XDP_OBS20	XDP_OBS20 - @k2_lib.K2	13B6
XDP_PWRGD	XDP_PWRGD - @k2_lib.K2	13C6
XDP_TCK	XDP_TCK - @k2_lib.K2	10A7 10C6 13B6 100A3
XDP_TDI	XDP_TDI - @k2_lib.K2	10B7 10C6 13B3 100A3
XDP_TDO	XDP_TDO - @k2_lib.K2	10A7 10C6 13B3 100A3
XDP_TMS	XDP_TMS - @k2_lib.K2	10B7 10C6 13B3 100A3
XDP_TRST_L	XDP_TRST_L - @k2_lib.K2	10A7 10C6 13B3 100A3
YUKON_RSET	YUKON_RSET - @k2_lib.K2	37C2
YUKON_VPD_CLK	YUKON_VPD_CLK - @k2_lib.K2	37B2
YUKON_VPD_DATA	YUKON_VPD_DATA - @k2_lib.K2	37B2

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Design: k2
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C600	CAP_402	k2[6D7]
C623	CAP_805	k2[6D7]
C624	CAP_1210	k2[6D8]
C625	CAP_P_6.3X5.5-SM	k2[6D8]
C626	CAP_402	k2[6D8]
C627	CAP_402	k2[6D8]
C628	CAP_402	k2[6D6]
C629	CAP_402	k2[6D7]
C630	CAP_402	k2[6D6]
C631	CAP_402	k2[6D6]
C1000	CAP_402	k2[10B5]
C1200	CAP_805	k2[12D7]
C1201	CAP_805	k2[12D6]
C1202	CAP_805	k2[12D6]
C1203	CAP_805	k2[12D6]
C1204	CAP_805	k2[12D6]
C1205	CAP_805	k2[12D5]
C1206	CAP_805	k2[12D5]
C1207	CAP_805	k2[12D5]
C1208	CAP_805	k2[12D4]
C1209	CAP_805	k2[12D4]
C1210	CAP_805	k2[12C7]
C1211	CAP_805	k2[12C6]
C1212	CAP_805	k2[12C6]
C1213	CAP_805	k2[12C6]
C1214	CAP_805	k2[12C6]
C1215	CAP_805	k2[12C5]
C1216	CAP_805	k2[12C5]
C1217	CAP_805	k2[12C5]
C1218	CAP_805	k2[12C4]
C1219	CAP_805	k2[12C4]
C1220	CAP_805	k2[12C7]
C1221	CAP_805	k2[12C6]
C1222	CAP_805	k2[12C6]
C1223	CAP_805	k2[12C6]
C1224	CAP_805	k2[12C6]
C1225	CAP_805	k2[12C5]
C1226	CAP_805	k2[12B7]
C1227	CAP_805	k2[12B6]
C1228	CAP_805	k2[12B6]
C1229	CAP_805	k2[12B6]
C1230	CAP_805	k2[12B6]
C1231	CAP_805	k2[12B5]
C1235	CAP_P_6.3X8-SM	k2[12A3]
C1236	CAP_402	k2[12A2]
C1237	CAP_402	k2[12A2]
C1238	CAP_402	k2[12A2]
C1239	CAP_402	k2[12A2]
C1240	CAP_402	k2[12A1]
C1241	CAP_402	k2[12A1]
C1250	CAP_P_CASE-D2-SM1	k2[12B7]
C1251	CAP_P_CASE-D2-SM1	k2[12B6]
C1252	CAP_P_CASE-D2-SM1	k2[12B5]
C1253	CAP_P_CASE-D2-SM1	k2[12B5]
C1254	CAP_P_CASE-D2-SM1	k2[12B6]
C1255	CAP_P_CASE-D2-SM1	k2[12B5]
C1280	CAP_603	k2[12B3]
C1281	CAP_402	k2[12B2]
C1300	CAP_402	k2[13B5]
C1301	CAP_402	k2[13B4]
C1410	CAP_402	k2[14A6]
C1425	CAP_402	k2[14A7]
C1615	CAP_402	k2[16C3]
C1616	CAP_402	k2[16C3]
C1622	CAP_603	k2[16C1]
C1623	CAP_402	k2[16C1]
C1624	CAP_603	k2[16C1]
C1625	CAP_402	k2[16C1]
C1640	CAP_402	k2[16A3]
C1801	CAP_402	k2[18A4]
C1802	CAP_402	k2[18A4]
C1803	CAP_402	k2[18A4]
C1804	CAP_402	k2[18A4]
C1805	CAP_402	k2[18A5]
C1806	CAP_402	k2[18A5]
C1807	CAP_402	k2[18A5]
C1911	CAP_402	k2[19A3]
C1912	CAP_402	k2[19A3]
C1913	CAP_402	k2[19A3]
C2100	CAP_P_6.3X8-SM	k2[21D7]
C2101	CAP_805	k2[21D7]
C2102	CAP_402	k2[21D7]
C2103	CAP_402	k2[21D6]
C2104	CAP_402	k2[21D6]
C2110	CAP_805	k2[21C7]
C2111	CAP_402	k2[21C7]
C2112	CAP_402	k2[21C7]
C2113	CAP_402	k2[21C6]
C2114	CAP_402	k2[21C6]
C2115	CAP_402	k2[21C6]
C2120	CAP_P_6.3X8-SM	k2[21C7]
C2121	CAP_603	k2[21C7]
C2122	CAP_603	k2[21C7]
C2123	CAP_603	k2[21C6]
C2124	CAP_402	k2[21C6]
C2130	CAP_P_6.3X8-SM	k2[21C7]
C2131	CAP_805	k2[21C7]
C2132	CAP_805	k2[21C7]
C2135	CAP_402	k2[21C7]
C2140	CAP_P_6.3X8-SM	k2[21B7]
C2141	CAP_805	k2[21B7]
C2142	CAP_805	k2[21B6]
C2143	CAP_603	k2[21B6]
C2144	CAP_402-1	k2[21B6]
C2145	CAP_805	k2[21B6]
C2146	CAP_603	k2[21B6]
C2148	CAP_402	k2[21B6]
C2150	CAP_805	k2[21A7]
C2151	CAP_402-1	k2[21A6]
C2160	CAP_402	k2[21A7]
C2161	CAP_402	k2[21A7]
C2165	CAP_402	k2[21A7]
C2170	CAP_603	k2[21D4]
C2171	CAP_402-1	k2[21D4]
C2173	CAP_P_SM-CASE-C1	k2[21C4]
C2174	CAP_603	k2[21C4]
C2177	CAP_603	k2[21C4]
C2180	CAP_402	k2[21D2]
C2181	CAP_805	k2[21D2]
C2182	CAP_402	k2[21D2]
C2183	CAP_805	k2[21C3]
C2184	CAP_402	k2[21C2]
C2190	CAP_603	k2[21B4]
C2191	CAP_402	k2[21B3]
C2192	CAP_402	k2[21B3]
C2195	CAP_603	k2[21A4]
C2196	CAP_805	k2[21A3]
C2197	CAP_402	k2[21A3]
C2200	CAP_402	k2[22B2]
C2201	FILTER_3P_A_NFM18	k2[22B2]
C2213	CAP_603	k2[22B2]
C2500	CAP_402	k2[25C2]
C2501	CAP_402	k2[25B2]
C2600	CAP_402	k2[26A3]
C2601	CAP_402	k2[26A3]
C2700	CAP_P_SM-CASE-C1	k2[27C7]
C2701	CAP_402	k2[27A6]
C2702	CAP_402	k2[27B1]
C2703	CAP_402-1	k2[27C8]
C2704	CAP_402	k2[27D8]
C2705	CAP_805	k2[27C7]
C2706	CAP_805	k2[27C7]
C2707	CAP_603	k2[27C7]
C2708	CAP_603	k2[27A6]
C2711	CAP_402	k2[27D1]
C2712	CAP_402	k2[27C1]
C2714	CAP_402	k2[27D1]
C2715	CAP_402	k2[27C1]
C2717	CAP_402	k2[27A6]
C2718	CAP_402	k2[27B1]
C2719	CAP_402	k2[27D3]
C2721	CAP_402	k2[27B3]
C2722	CAP_402	k2[27B1]
C2723	CAP_402	k2[27B1]
C2724	CAP_603	k2[27B1]
C2725	CAP_402	k2[27D3]
C2726	CAP_402	k2[27C3]
C2727	CAP_402	k2[27C3]
C2728	CAP_402	k2[27C3]
C2729	CAP_402	k2[27D5]
C2730	CAP_402	k2[27D5]
C2731	CAP_402	k2[27D5]
C2732	CAP_603	k2[27B7]
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C2734	CAP_402	k2[27D5]
C2735	CAP_603	k2[27A6]
C2736	CAP_603	k2[27B7]
C2737	CAP_402	k2[27C3]
C2738	CAP_402	k2[27C3]
C2739	CAP_805	k2[27C1]
C2741	CAP_402	k2[27B3]
C2805	CAP_402	k2[28D5]
C2808	CAP_402	k2[28C6]
C2809	CAP_402	k2[28C6]
C2810	CAP_402	k2[28D6]
C2811	CAP_402	k2[28A7]
C2900	CAP_402	k2[29D7]
C2901	CAP_603	k2[29D6]
C2902	CAP_402	k2[29D6]
C2903	CAP_402	k2[29D6]
C2904	CAP_402	k2[29D5]
C2905	CAP_402	k2[29D5]
C2906	CAP_402	k2[29D5]
C2907	CAP_603	k2[29C5]
C2908	CAP_402	k2[29C5]
C2909	CAP_402	k2[29D4]
C2910	CAP_603	k2[29D3]
C2911	CAP_402	k2[29D2]
C2912	CAP_402	k2[29D4]
C2913	CAP_402	k2[29D3]
C2914	CAP_603	k2[29D3]
C2915	CAP_402	k2[29C4]
C2916	CAP_603	k2[29C3]
C2989	CAP_402	k2[29C6]
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C3101	CAP_603	k2[31B2]
C3110	CAP_402	k2[31B2]
C3111	CAP_402	k2[31B2]
C3112	CAP_402	k2[31B1]
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C3121	CAP_402	k2[31B1]
C3122	CAP_402	k2[31A1]
C3123	CAP_402	k2[31A1]
C3130	CAP_603	k2[31D6]
C3131	CAP_402	k2[31D6]
C3140	CAP_603	k2[31A7]
C3141	CAP_402	k2[31A6]
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C3201	CAP_603	k2[32B2]
C3210	CAP_402	k2[32B2]
C3211	CAP_402	k2[32B2]
C3212	CAP_402	k2[32B1]
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C3214	CAP_402	k2[32B2]
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C3221	CAP_402	k2[32B1]
C3222	CAP_402	k2[32A1]
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C3230	CAP_603	k2[32D6]
C3231	CAP_402	k2[32D6]
C3240	CAP_603	k2[32A6]
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C3300	CAP_402	k2[33D4]
C3302	CAP_402	k2[33D4]
C3305	CAP_402	k2[33D4]
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C3714	CAP_402	k2[37D5]
C3715	CAP_402	k2[37D4]
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C3731	CAP_402	k2[37C7]
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C3742	CAP_402	k2[37B6]
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C3751	CAP_402	k2[37B5]
C3780	CAP_402	k2[37B2]
C3800	CAP_805	k2[38C6]
C3801	CAP_402	k2[38C6]
C3802	CAP_805	k2[38C6]
C3803	CAP_603	k2[38C5]
C3804	CAP_402	k2[38C5]
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C3811	CAP_402	k2[38B6]
C3812	CAP_805	k2[38B6]
C3813	CAP_603	k2[38B5]
C3814	CAP_402	k2[38B5]
C3815	CAP_603	k2[38A4]
C3816	CAP_402	k2[38A4]
C3900	CAP_402	k2[39D7]
C3901	CAP_402	k2[39D7]
C3902	CAP_402	k2[39D6]
C3903	CAP_402	k2[39D6]
C3910	CAP_1808	k2[39A3]
C4000	CAP_402	k2[40B7]
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C4010	CAP_402	k2[40C2]
C4011	CAP_402	k2[40C2]
C4020	CAP_402	k2[40C3]
C4021	CAP_402	k2[40C3]
C4090	CAP_402	k2[40B6]
C4200	CAP_402-LF	k2[42C7]
C4201	CAP_402-LF	k2[42C7]
C4210	CAP_402	k2[42C6]
C4211	CAP_402	k2[42C5]
C4212	CAP_805-1	k2[42C5]
C4213	CAP_805-1	k2[42C5]
C4230	CAP_402	k2[42A5]
C4231	CAP_402	k2[42A5]
C4240	CAP_402	k2[42A7]
C4241	CAP_402	k2[42A7]
C4242	CAP_402	k2[42A7]
C4250	CAP_402	k2[42B7]
C4251	CAP_402	k2[42B7]
C4252	CAP_402	k2[42B7]
C4253	CAP_402	k2[42B6]
C4254	CAP_402	k2[42B6]
C4260	CAP_402	k2[42B7]
C4261	CAP_402	k2[42B7]
C4262	CAP_402	k2[42B7]
C4263	CAP_402	k2[42B6]
C4264	CAP_402	k2[42B6]
C4265	CAP_402	k2[42B6]
C4266	CAP_402	k2[42B6]
C4280	CAP_402	k2[42A6]
C4281	CAP_402	k2[42A6]
C4290	CAP_402	k2[42B5]
C4291	CAP_402	k2[42B5]
C4300	CAP_603-1	k2[43D3]
C4301	CAP_603-1	k2[43B3]
C4310	CAP_402	k2[43D4]
C4311	CAP_402	k2[43D4]
C4312	CAP_402	k2[43C4]
C4313	CAP_402	k2[43C4]
C4320	CAP_402	k2[43B5]
C4321	CAP_402	k2[43B5]
C4322	CAP_402	k2[43A5]
C4323	CAP_402	k2[43A5]
C4332	CAP_402	k2[43C2]
C4335	CAP_603-1	k2[43C2]
C4350	CAP_402	k2[43C7]
C4354	CAP_402	k2[43B7]
C4360	CAP_402	k2[43D7]
C4364	CAP_402	k2[43B7]
C4404	CAP_402	k2[44B6]
C4405	CAP_402	k2[44B3]
C4406	CAP_805	k2[44B3]
C4510	CAP_402	k2[45D6]
C4511	CAP_402	k2[45D6]
C4515	CAP_402	k2[45C6]
C4516	CAP_402	k2[45C6]
C4600	CAP_P_CASE-D2-LF	k2[46C8]
C4601	CAP_402	k2[46C8]
C4602	CAP_402	k2[46C7]
C4603	CAP_402	k2[46C7]
C4604	CAP_402	k2[46D8]
C4605	CAP_402	k2[46D7]
C4613	CAP_402	k2[46D2]
C4623	CAP_402	k2[46C5]
C4633	CAP_402	k2[46A5]
C4650	CAP_402	k2[46D5]
C4700	CAP_805-1	k2[47D7]
C4701	CAP_402	k2[47D6]
C4720	CAP_805-1	k2[47D3]
C4721	CAP_402	k2[47D3]
C4781	CAP_402	k2[47A2]
C4902	CAP_805	k2[49D4]
C4903	CAP_402	k2[49D4]
C4904	CAP_402	k2[49D3]
C4905	CAP_402	k2[49D3]
C4906	CAP_402	k2[49D3]
C4907	CAP_402	k2[49D2]
C4920	CAP_402	k2[49C3]
C5000	CAP_402	k2[50D7]
C5001	CAP_402	k2[50D7]
C5010	CAP_402	k2[50C6]
C5020	CAP_402	k2[50C7]
C5021	CAP_402	k2[50C7]
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C5066	CAP_603	k2[50B7]
C5067	CAP_402	k2[50B7]
C5309	CAP_402	k2[53D6]
C5359	CAP_402	k2[53D3]
C5370	CAP_402	k2[53C7]
C5380	CAP_402	k2[53C5]
C5381	CAP_402	k2[53C4]
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C5384	CAP_402	k2[53B1]
C5386	CAP_402	k2[53A4]
C5388	CAP_402	k2[53A3]
C5500	CAP_402	k2[55C7]
C5501	CAP_402	k2[55B4]
C5502	CAP_805-1	k2[55B4]
C5503	CAP_402	k2[55B4]
C5510	CAP_402	k2[55A7]
C5511	CAP_402	k2[55A6]
C5550	CAP_402	k2[55B7]
C5551	CAP_402	k2[55B6]
C5560	CAP_402	k2[55C5]
C5570	CAP_402	k2[55D3]
C5580	CAP_402	k2[55C4]
C5601	CAP_805	k2[56D5]
C5602	CAP_P_6.3X5.5SM1	k2[56C4]
C5603	CAP_805	k2[56B5]
C5605	CAP_P_6.3X5.5SM1	k2[56B3]
C5701	CAP_805	k2[57C5]
C5702	CAP_P_6.3X5.5SM1	k2[57C3]
C6100	CAP_402	k2[61C4]
C7000	CAP_402	k2[70C6]
C7001	CAP_402	k2[70C6]
C7002	CAP_402	k2[70C6]
C7003	CAP_402	k2[70C6]
C7010	CAP_603	k2[70D6]
C7052	CAP_402	k2[70D2]
C7056	CAP_402	k2[70D1]
C7060	CAP_402	k2[70A5]
C7061	CAP_402	k2[70B5]
C7062	CAP_402	k2[70B5]
C7090	CAP_402	k2[70A3]
C7100	CAP_402	k2[71C4]
C7101	CAP_1206-1	k2[71D1]
C7102	CAP_402	k2[71B4]
C7103	CAP_402	k2[71C2]
C7104	CAP_402	k2[71B2]
C7105	CAP_402	k2[71C8]
C7106	CAP_402	k2[71B8]
C7107	CAP_402	k2[71B7]
C7108	CAP_1206-1	k2[71D1]
C7109	CAP_P_TH	k2[71D5]
C7110	CAP_402	k2[71C7]
C7111	CAP_402	k2[71B2]
C7112	CAP_402	k2[71C2]
C7113	CAP_402	k2[71B7]
C7114	CAP_402	k2[71B8]
C7115	CAP_603	k2[71D4]
C7116	CAP_402	k2[71B4]
C7121	CAP_402	k2[71A5]
C7126	CAP_603-1	k2[71D6]
C7127	CAP_603	k2[71C4]
C7128	CAP_402	k2[71B4]
C7129	CAP_402	k2[71B5]
C7130	CAP_402	k2[71D6]
C7131	CAP_402	k2[71B5]
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C7133	CAP_402	k2[71A5]
C7134	CAP_402	k2[71B5]
C7135	CAP_603	k2[71D4]
C7136	CAP_603	k2[71C4]
C7145	CAP_402	k2[71D1]
C7146	CAP_402	k2[71C1]
C7147	CAP_402	k2[71D3]
C7148	CAP_402	k2[71C3]
C7150	CAP_1206-1	k2[71D4]
C7152	CAP_1206-1	k2[71D4]
C7154	CAP_P_TH	k2[71D2]
C7155	CAP_1206-1	k2[71D1]
C7156	CAP_1206-1	k2[71D4]
C7190	CAP_402	k2[71C3]
C7192	CAP_402	k2[71B3]
C7196	CAP_402	k2[71D6]
C7200	CAP_402	k2[72C4]
C7201	CAP_1206-1	k2[72D2]
C7203	CAP_402	k2[72C2]
C7208	CAP_1206-1	k2[72D2]
C7212	CAP_402	k2[72C3]
C7215	CAP_603	k2[72C5]

C7235	CAP_603	k2[72D6]
C7245	CAP_402	k2[72C2]
C7247	CAP_402	k2[72D4]
C7254	CAP_P_TH	k2[72D2]
C7255	CAP_1206-1	k2[72D2]
C7290	CAP_402	k2[72C4]
C7300	CAP_P_CASE-D2-SM	k2[73C8]
C7301	CAP_805	k2[73B8]
C7302	CAP_402	k2[73B7]
C7303	CAP_805	k2[73C7]
C7304	CAP_805	k2[73C8]
C7305	CAP_805	k2[73C7]
C7310	CAP_603	k2[73C7]
C7324	CAP_402	k2[73B7]
C7330	CAP_603-1	k2[73D6]
C7331	CAP_603	k2[73C6]
C7332	CAP_402	k2[73B5]
C7335	CAP_402	k2[73B6]
C7340	CAP_P_TH	k2[73D7]
C7341	CAP_1206-1	k2[73D7]
C7342	CAP_1206-1	k2[73D6]
C7345	CAP_402	k2[73B3]
C7360	CAP_603	k2[73D2]
C7361	CAP_603	k2[73C2]
C7364	CAP_402	k2[73B2]
C7370	CAP_402	k2[73B2]
C7372	CAP_402	k2[73B4]
C7381	CAP_1206-1	k2[73D2]
C7382	CAP_1206-1	k2[73D2]
C7390	CAP_P_CASE-D2-SM	k2[73C1]
C7391	CAP_P_CASE-D2-SM	k2[73C2]
C7392	CAP_805	k2[73C1]
C7393	CAP_805	k2[73C1]
C7400	CAP_P_CASE-D2-SM	k2[74C8]
C7401	CAP_805	k2[74C8]
C7402	CAP_402	k2[74B7]
C7403	CAP_P_CASE-D2-SM	k2[74C7]
C7404	CAP_805	k2[74C8]
C7410	CAP_603	k2[74C7]
C7424	CAP_402	k2[74B7]
C7430	CAP_603-1	k2[74D6]
C7431	CAP_603	k2[74C6]
C7432	CAP_402	k2[74B5]
C7435	CAP_402	k2[74B6]
C7440	CAP_P_TH	k2[74D7]
C7441	CAP_1206-1	k2[74D7]
C7442	CAP_1206-1	k2[74D6]
C7445	CAP_402	k2[74B3]
C7460	CAP_603-1	k2[74D2]
C7461	CAP_603	k2[74C2]
C7464	CAP_402	k2[74B2]
C7470	CAP_402	k2[74B2]
C7472	CAP_402	k2[74B4]
C7480	CAP_P_TH	k2[74D3]
C7481	CAP_1206-1	k2[74D2]
C7482	CAP_1206-1	k2[74D2]
C7490	CAP_P_TH1	k2[74C2]
C7491	CAP_P_TH1	k2[74C1]
C7492	CAP_805	k2[74C1]
C7493	CAP_805	k2[74C1]
C7500	CAP_603	k2[75D5]
C7501	CAP_603	k2[75D6]
C7502	CAP_603	k2[75D6]
C7503	CAP_402	k2[75C2]
C7506	CAP_402	k2[75C8]
C7507	CAP_402	k2[75C6]
C7508	CAP_603	k2[75C7]
C7509	CAP_402	k2[75D4]
C7510	CAP_402	k2[75C5]
C7530	CAP_P_TH	k2[75D5]
C7531	CAP_603	k2[75D4]
C7532	CAP_P_TH	k2[75D5]
C7533	CAP_1206-1	k2[75D5]
C7534	CAP_1206-1	k2[75D4]
C7540	CAP_805	k2[75C3]
C7541	CAP_805	k2[75C3]
C7542	CAP_P_CASE-D2-SM	k2[75C2]
C7543	CAP_P_CASE-D2-SM	k2[75C2]
C7544	CAP_P_CASE-D2-SM	k2[75C2]
C7545	CAP_402	k2[75D3]
C7547	CAP_402	k2[75D7]
C7550	CAP_402	k2[75B4]
C7551	CAP_805-1	k2[75A6]
C7552	CAP_805-1	k2[75A4]
C7553	CAP_402	k2[75A6]
C7555	CAP_P_CASE-C3	k2[75A4]
C7559	CAP_603	k2[75B5]
C7560	CAP_402	k2[75D8]
C7564	CAP_402	k2[75C3]
C7585	CAP_402	k2[75B3]
C7586	CAP_402	k2[75B2]
C7587	CAP_402	k2[75B2]
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C7595	CAP_402	k2[75B3]
C7596	CAP_402	k2[75B2]
C7597	CAP_402	k2[75B2]
C7598	CAP_402	k2[75B2]
C7599	CAP_402	k2[75B1]
C7600	CAP_603	k2[76C4]
C7601	CAP_603	k2[76A4]
C7602	CAP_402	k2[76A4]
C7604	CAP_402	k2[76A3]
C7605	CAP_402	k2[76B5]
C7607	CAP_402	k2[76A3]
C7608	CAP_402	k2[76D2]
C7609	CAP_402	k2[76D7]
C7612	CAP_603	k2[76A7]
C7613	CAP_402	k2[76A7]
C7621	CAP_402	k2[76B6]
C7622	CAP_402	k2[76C5]
C7624	CAP_402	k2[76C6]
C7625	CAP_402	k2[76B6]
C7626	CAP_402	k2[76B6]
C7628	CAP_402	k2[76B7]
C7629	CAP_402	k2[76B7]
C7630	CAP_402	k2[76A5]
C7631	CAP_402	k2[76C7]
C7632	CAP_402	k2[76C2]

C7640	CAP_1206-1	k2[76D6]
C7641	CAP_1206-1	k2[76D6]
C7642	CAP_1206-1	k2[76D6]
C7643	CAP_1206-1	k2[76D6]
C7650	CAP_805	k2[76B7]
C7651	CAP_P_CASE-D3L	k2[76B8]
C7652	CAP_805	k2[76B8]
C7653	CAP_805	k2[76C8]
C7654	CAP_805	k2[76C8]
C7661	CAP_402	k2[76B3]
C7662	CAP_402	k2[76C4]
C7664	CAP_402	k2[76C3]
C7665	CAP_402	k2[76B4]
C7666	CAP_402	k2[76B3]
C7668	CAP_402	k2[76B2]
C7669	CAP_402	k2[76B2]
C7670	CAP_402	k2[76B4]
C7680	CAP_1206-1	k2[76D3]
C7681	CAP_1206-1	k2[76D4]
C7682	CAP_P_SM-1	k2[76D4]
C7689	CAP_402	k2[76B4]
C7690	CAP_805	k2[76B2]
C7691	CAP_P_CASE-D3L	k2[76B1]
C7692	CAP_P_CASE-D3L	k2[76B1]
C7693	CAP_P_CASE-D3L	k2[76B1]
C7700	CAP_805	k2[77B5]
C7705	CAP_805	k2[77B5]
C7706	CAP_603	k2[77B4]
C7710	CAP_805	k2[77D6]
C7712	CAP_402-1	k2[77D4]
C7715	CAP_805	k2[77D3]
C7800	CAP_402	k2[78D2]
C7801	CAP_402	k2[78D2]
C7810	CAP_402	k2[78D6]
C7811	CAP_402	k2[78D6]
C7850	CAP_402	k2[78B2]
C7851	CAP_402	k2[78C2]
C7895	CAP_402	k2[78B7]
C7896	CAP_402	k2[78B5]
C7899	CAP_402	k2[78C6]
C8400	CAP_P_SM-LF	k2[84C5]
C8401	CAP_805	k2[84C7]
C8410	CAP_402	k2[84C7]
C8411	CAP_402	k2[84C7]
C8412	CAP_402	k2[84C5]
C8413	CAP_402	k2[84C4]
C8420	CAP_402	k2[84C7]
C8421	CAP_402	k2[84C7]
C8422	CAP_402	k2[84C7]
C8423	CAP_402	k2[84C7]
C8424	CAP_402	k2[84B7]
C8425	CAP_402	k2[84B7]
C8426	CAP_402	k2[84B7]
C8427	CAP_402	k2[84B7]
C8428	CAP_402	k2[84B7]
C8429	CAP_402	k2[84B7]
C8430	CAP_402	k2[84B7]
C8431	CAP_402	k2[84B7]
C8432	CAP_402	k2[84B7]
C8433	CAP_402	k2[84B7]
C8434	CAP_402	k2[84B7]
C8435	CAP_402	k2[84B7]
C8436	CAP_402	k2[84B7]
C8437	CAP_402	k2[84B7]
C8438	CAP_402	k2[84B7]
C8439	CAP_402	k2[84B7]
C8440	CAP_402	k2[84B7]
C8441	CAP_402	k2[84A7]
C8442	CAP_402	k2[84A7]
C8443	CAP_402	k2[84A7]
C8444	CAP_402	k2[84A7]
C8445	CAP_402	k2[84A7]
C8446	CAP_402	k2[84A7]
C8447	CAP_402	k2[84A7]
C8448	CAP_402	k2[84A7]
C8449	CAP_402	k2[84A7]
C8450	CAP_402	k2[84A7]
C8451	CAP_402	k2[84A7]
C8500	CAP_805	k2[85A5]
C8510	CAP_402	k2[85A4]
C8511	CAP_402	k2[85A4]
C8570	CAP_402	k2[85D2]
C9000	CAP_603-1	k2[90C7]
C9001	CAP_402	k2[90C5]
C9010	CAP_402	k2[90A8]
C9020	CAP_1210	k2[90C5]
C9130	CAP_402	k2[91B7]
C9131	CAP_805-1	k2[91B7]
C9140	CAP_402	k2[91A5]
C9141	CAP_402	k2[91B5]
C9142	CAP_402	k2[91B5]
C9143	CAP_402	k2[91A6]
C9144	CAP_402	k2[91B6]
C9145	CAP_402	k2[91B6]
C9160	CAP_402	k2[91B4]
C9161	CAP_402	k2[91B4]
C9162	CAP_402	k2[91A2]
C9163	CAP_402	k2[91A2]
C9410	CAP_603	k2[94C3]
C9411	CAP_402	k2[94D3]
C9413	CAP_402	k2[94C2]
C9414	CAP_402	k2[94C2]
C9800	CAP_805	k2[98C5]
C9801	CAP_402	k2[98C4]
C9802	CAP_402	k2[98C4]
D2185	DIODE_SCHOT_SOT23	k2[21C4]
D2186	DIODE_SCHOT_SOT23	k2[21B4]
D2702	DIODE_SCHOT_6PB_SOT-363	k2[27D8 27D8]
D2800	DIODE_SCHOT_6PB_SOT-363	k2[28D6]
D4390	ZENER_SOT23	k2[43A6]
D4600	DIODE_SCHOT_3P_A_SC-75	k2[46C2]
D4601	DIODE_SCHOT_3P_A_SC-75	k2[46B5]
D4602	DIODE_SCHOT_3P_A_SC-75	k2[46A5]
D5600	DIODE_SOT23	k2[56C4]
D5601	DIODE_SOT23	k2[56B4]
D5700	DIODE_SOT23	k2[57C4]
D7100	DIODE_SCHOT_SMB	k2[71D2]
D7101	DIODE_SCHOT_SMB	k2[71B2]
D7200	DIODE_SCHOT_SMB	k2[72C3]

D7300	DIODE_SCHOT_5P_TLM83 3	k2[73B6]
D7301	DIODE_SCHOT_SOT23	k2[73C6]
D7373	DIODE_SCHOT_5P_TLM83 3	k2[73B3]
D7374	DIODE_SCHOT_SOT23	k2[73C3]
D7400	DIODE_SCHOT_5P_TLM83 3	k2[74B6]
D7401	DIODE_SCHOT_SOT23	k2[74C6]
D7473	DIODE_SCHOT_5P_TLM83 3	k2[74B3]
D7474	DIODE_SCHOT_SOT23	k2[74C4]
D7520	DIODE_SCHOT_5P_TLM83 3	k2[75C4]
D7600	DIODE_SCHOT_5P_TLM83 3	k2[76B7]
D7601	DIODE_SCHOT_5P_TLM83 3	k2[76B2]
D7624	DIODE_SCHOT_SOD-323	k2[76C6]
D7664	DIODE_SCHOT_SOD-323	k2[76C3]
D7750	DIODE_SCHOT_SOD-123	k2[77B5]
D7810	DIODE_SCHOT_SOD-123	k2[78C6]
D9400	ZENER_CASE425	k2[94C1]
D9410	DIODE_SCHOT_SOD-123	k2[94D6]
DE4300	DIODE_SCHOT_SM	k2[43D7]
DP4310	DIODE_DUAL_6P_SOT-36 3	k2[43D4 43D3]
DP4311	DIODE_DUAL_6P_SOT-36 3	k2[43C4 43C3]
DP4320	DIODE_DUAL_6P_SOT-36 3	k2[43B5 43B4]
DP4321	DIODE_DUAL_6P_SOT-36 3	k2[43A5 43A4]
DS4599	LED_2.0X1.25MM-SM	k2[45C2]
F4300	FUSE_SM	k2[43D6]
F4310	FUSE_SM	k2[43D6]
F9410	FUSE_805	k2[94D5]
FL4300	FILTER_4P_L701-SM	k2[43B3]
FL4310	FILTER_4P_L701-SM	k2[43B3]
J600	CON_M12RT_D_THB_M-RT -TH	k2[6D7]
J1000	MEROM_BGA-SKT-P	k2[10C3 10D7]
J1000	MEROM_BGA-SKT-P	k2[11D3 11D7]
J1300	CON_F60ST_D_SM1_F-ST -SM	k2[13C4]
J2800	BATTERY_2P_SM	k2[28D8]
J3100	CON_F200RT_DDR2DIMM_ 5MT_SM_F-RT-SM	k2[31D5]
J3200	CON_F200RT_DDR2DIMM_ 5MT_SM_F-RT-SM	k2[32D5]
J3400	CON_F52RT_D2MT_SM_F- RT-SM	k2[34C5]
J3900	CON_RJ45_8ANG_D3MT_T H_F-ANG-TH	k2[39C3]
J4300	CON_F9ANG_1394B_D6MT _TH_F-ANG-TH1	k2[43C2]
J4301	CON_F6ANG_S3MT_1394A _TH_F-ANG-TH	k2[43B2]
J4401	CON_M50RT_D2MT_SM_M- RT-SM	k2[44C4]
J4510	CON_M7ST_SATA_SM_M-S T-SM	k2[45D7]
J4610	CON_F4ANG_S4MT_USB_T H_F-ANG-TH1	k2[46D1]
J4620	CON_F4ANG_S4MT_USB_T H_F-ANG-TH1	k2[46B4]
J4630	CON_F4ANG_S4MT_USB_T H_F-ANG-TH1	k2[46A4]
J4700	CON_M5ST_S2MT_SM_M-S T-SM	k2[47B5]
J4720	CON_M4ST_S2MT_SM_M-S T-SM	k2[47D2]
J4780	CON_M4ST_S2MT_SM_M-S T-SM	k2[47B2]
J5010	CON_M2ST_S2MT_SM_M-S T-SM	k2[50C6]
J5100	CON_F30STSM_5047_SM1	k2[51B5]
J5500	CON_M5ST_S2MT_SM_PN1 VD_M-ST-SM	k2[55D7]
J5510	CON_M2ST_S2MT_SM_M-S T-SM	k2[55A7]
J5511	CON_M2RT_S2MT_SM_M-R T-SM	k2[55A5]
J5550	CON_M3RT_S2MT_SM_M-R T-SM	k2[55B7]
J5551	CON_M2RT_S2MT_SM_M-R T-SM1	k2[55B5]
J5560	CON_M5ST_S2MT_SM_PN1 VD_M-ST-SM	k2[55D6]
J5600	CON_M4ST_S2MT_SM_M-S T-SM	k2[56D3]
J5601	CON_M4RT_S2MT_SM_M-R T-SM2	k2[56B2]
J5700	CON_M4ST_S2MT_SM_M-S T-SM	k2[57C2]
J8400	CON_F230RT_MXM_SM1_F -RT-SM	k2[84C5]
J8400	CON_F230RT_MXM_SM1_F -RT-SM	k2[85C6]
J9002	CON_F30ST_D_SM_F-ST-SM	k2[90B7]
J9410	CON_DVI_F32ST_Q2MT_S M_F-ST-SM1	k2[94D5]
J9800	CON_F22RT_S2MT_SM_F-RT-SM	k2[98C5]
L2150	IND_0603	k2[21A7]
L2173	IND_1210	k2[21D4]
L2181	IND_0603	k2[21D2]
L2183	IND_0603	k2[21C2]
L2190	IND_0805	k2[21B3]
L2195	IND_0805	k2[21A3]
L2700	IND_0805-1	k2[27C8]
L2702	IND_0805	k2[27A7]
L2703	IND_1210	k2[27A7]
L2901	IND_0402	k2[29D7]
L2902	IND_0402	k2[29D3]
L2903	IND_0402	k2[29C7]
L3800	IND_0805-1	k2[38C6]
L3810	IND_0805-1	k2[38B6]
L4200	IND_0402-LF	k2[42D5]
L4210	IND_0402-LF	k2[42B2]
L4211	IND_0402-LF	k2[42B2]
L4300	IND_SM	k2[43D3]
L4301	IND_SM	k2[43B4]

L4610	IND_SM	k2[46D3]
L4612	FILTER_4P_L701-SM	k2[46D3]
L4620	IND_SM	k2[46C6]
L4622	FILTER_4P_L701-SM	k2[46B6]
L4630	IND_SM	k2[46B6]
L4632	FILTER_4P_L701-SM	k2[46A6]
L4700	IND_SM	k2[47D6]
L4701	FILTER_4P_L701-SM	k2[47B6]
L4710	FILTER_4P_L701-SM	k2[47A6]
L7100	IND_MSQ1211R36LE-TH	k2[71D2]
L7101	IND_MSQ1211R36LE-TH	k2[71B2]
L7200	IND_MSQ1211R36LE-TH	k2[72C3]
L7300	IND_MMD06EZ-SM	k2[73C7]
L7360	IND_MMD06EZ-SM	k2[73C2]
L7400	IND_MMD06EZ-SM	k2[74C7]
L7460	IND_IHLP5050-MMD12CE -SM	k2[74C2]
L7580	IND_MSQ12111R5LE-TH	k2[75C3]
L7620	IND_MMD06EZ-SM	k2[76B7]
L7680	IND_MSQ12113R0LE-TH	k2[76B2]
L7710	IND_IHLP	k2[77D4]
L9000	IND_SM	k2[90C6]
L9140	IND_0402	k2[91A5]
L9141	IND_0402	k2[91B5]
L9142	IND_0402	k2[91B5]
L9160	IND_0402	k2[91B2]
L9161	IND_0402	k2[91A2]
L9400	FILTER_4P_SM	k2[94D7]
L9401	FILTER_4P_SM	k2[94D7]
L9402	FILTER_4P_SM	k2[94C7]
L9403	FILTER_4P_SM	k2[94B7]
L9410	IND_SM-1	k2[94D4]
LED601	LED_2.0X1.25MM-SM	k2[6A8]
LED602	LED_2.0X1.25MM-SM	k2[6A7]
LED603	LED_2.0X1.25MM-SM	k2[6A6]
LED604	LED_2.0X1.25MM-SM	k2[6B7]
LED3900	LED_2.0X1.25MM-SM	k2[39A7]
LED3901	LED_2.0X1.25MM-SM	k2[39A7]
LED3902	LED_2.0X1.25MM-SM	k2[39A7]
LED3903	LED_2.0X1.25MM-SM	k2[39A6]
LED4400	LED_2.0X1.25MM-SM	k2[44B5]
PP1000	PROBEPOINT_SM	k2[7D7]
PP1001	PROBEPOINT_SM	k2[7D7]
PP1002	PROBEPOINT_SM	k2[7D7]
PP1003	PROBEPOINT_SM	k2[7D7]
PP1004	PROBEPOINT_SM	k2[7D7]
PP1005	PROBEPOINT_SM	k2[7D7]
PP1006	PROBEPOINT_SM	k2[7D7]
PP1007	PROBEPOINT_SM	k2[7D7]
PP1008	PROBEPOINT_SM	k2[7D7]
PP1009	PROBEPOINT_SM	k2[7D7]
PP1010	PROBEPOINT_SM	k2[7D7]
PP1011	PROBEPOINT_SM	k2[7D7]
PP1012	PROBEPOINT_SM	k2[7D7]
PP1013	PROBEPOINT_SM	k2[7D7]
PP1014	PROBEPOINT_SM	k2[7D7]
PP1015	PROBEPOINT_SM	k2[7D7]
PP1016	PROBEPOINT_SM	k2[7D7]
PP1017	PROBEPOINT_SM	k2[7D7]
PP1018	PROBEPOINT_SM	k2[7D7]
PP1019	PROBEPOINT_SM	k2[7D7]
PP1020	PROBEPOINT_SM	k2[7D7]
PP1021	PROBEPOINT_SM	k2[7C7]
PP1022	PROBEPOINT_SM	k2[7C7]
PP1023	PROBEPOINT_SM	k2[7C7]
PP1024	PROBEPOINT_SM	k2[7C7]
PP1025	PROBEPOINT_SM	k2[7C7]
PP1026	PROBEPOINT_SM	k2[7C7]
PP1027	PROBEPOINT_SM	k2[7C7]
PP1028	PROBEPOINT_SM	k2[7C7]
PP1029	PROBEPOINT_SM	k2[7C7]
PP1030	PROBEPOINT_SM	k2[7C7]
PP1031	PROBEPOINT_SM	k2[7C7]
PP1032	PROBEPOINT_SM	k2[7C7]
PP1033	PROBEPOINT_SM	k2[7C7]
PP1034	PROBEPOINT_SM	k2[7C7]
PP1035	PROBEPOINT_SM	k2[7C7]
PP1400	PROBEPOINT_SM	k2[7D6]
PP1401	PROBEPOINT_SM	k2[7D6]
PP1402	PROBEPOINT_SM	k2[7D6]
PP1403	PROBEPOINT_SM	k2[7D6]
PP1404	PROBEPOINT_SM	k2[7D6]
PP1405	PROBEPOINT_SM	k2[7D6]
PP1406	PROBEPOINT_SM	k2[7D6]
PP1407	PROBEPOINT_SM	k2[7D6]
PP1408	PROBEPOINT_SM	k2[7D6]
PP1409	PROBEPOINT_SM	k2[7D6]
PP1410	PROBEPOINT_SM	k2[7D6]
PP1411	PROBEPOINT_SM	k2[7D6]
PP1412	PROBEPOINT_SM	k2[7D6]
PP1413	PROBEPOINT_SM	k2[7D6]
PP1414	PROBEPOINT_SM	k2[7D6]
PP1415	PROBEPOINT_SM	k2[7D6]
PP1416	PROBEPOINT_SM	k2[7D6]
PP1417	PROBEPOINT_SM	k2[7D6]
PP1418	PROBEPOINT_SM	k2[7D6]
PP1419	PROBEPOINT_SM	k2[7D6]
PP1420	PROBEPOINT_SM	k2[7D6]
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PP1422	PROBEPOINT_SM	k2[7C6]
PP1423	PROBEPOINT_SM	k2[7C6]
PP1424	PROBEPOINT_SM	k2[7C6]
PP1425	PROBEPOINT_SM	k2[7C6]
PP1426	PROBEPOINT_SM	k2[7C6]
PP1427	PROBEPOINT_SM	k2[7C6]
PP1428	PROBEPOINT_SM	k2[7C6]
PP1429	PROBEPOINT_SM	k2[7C6]
PP1430	PROBEPOINT_SM	k2[7C6]
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PP1432	PROBEPOINT_SM	k2[7C6]
PP1433	PROBEPOINT_SM	k2[7C6]
PP1434	PROBEPOINT_SM	k2[7C6]
PP1435	PROBEPOINT_SM	k2[7C6]
PP1436	PROBEPOINT_SM	k2[7C6]
PP1437	PROBEPOINT_SM	k2[7C6]
PP1438	PROBEPOINT_SM	k2[7C6]
PP1439	PROBEPOINT_SM	k2[7C6]
PP1440	PROBEPOINT_SM	k2[7C6]
PP1441	PROBEPOINT_SM	k2[7C6]
PP1442	PROBEPOINT_SM	k2[7C6]
PP1443	PROBEPOINT_SM	k2[7C6]
PP1444	PROBEPOINT_SM	k2[7B6]
PP1445	PROBEPOINT_SM	k2[7B6]
PP1446	PROBEPOINT_SM	k2[7B6]

PP1447	PROBEPOINT_SM	k2[7B6]
PP1448	PROBEPOINT_SM	k2[7B6]
PP1449	PROBEPOINT_SM	k2[7B6]
PP1450	PROBEPOINT_SM	k2[7B6]
PP1451	PROBEPOINT_SM	k2[7B6]
PP1452	PROBEPOINT_SM	k2[7B6]
PP1453	PROBEPOINT_SM	k2[7B6]
PP1454	PROBEPOINT_SM	k2[7B6]
PP1455	PROBEPOINT_SM	k2[7B6]
PP1456	PROBEPOINT_SM	k2[7B6]
PP1457	PROBEPOINT_SM	k2[7B6]
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PP1459	PROBEPOINT_SM	k2[7B6]
PP1460	PROBEPOINT_SM	k2[7B6]
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PP1462	PROBEPOINT_SM	k2[7B6]
PP1463	PROBEPOINT_SM	k2[7B6]
PP1464	PROBEPOINT_SM	k2[7B6]
PP1465	PROBEPOINT_SM	k2[7B6]
PP1466	PROBEPOINT_SM	k2[7B6]
PP1467	PROBEPOINT_SM	k2[7B6]
PP1468	PROBEPOINT_SM	k2[7B6]
PP1469	PROBEPOINT_SM	k2[7B6]
PP1470	PROBEPOINT_SM	k2[7A6]
PP1471	PROBEPOINT_SM	k2[7A6]
PP1472	PROBEPOINT_SM	k2[7A6]
PP1473	PROBEPOINT_SM	k2[7A6]
PP1474	PROBEPOINT_SM	k2[7A6]
PP1475	PROBEPOINT_SM	k2[7A6]
PP1476	PROBEPOINT_SM	k2[7A6]
PP1477	PROBEPOINT_SM	k2[7A6]
PP1478	PROBEPOINT_SM	k2[7A6]
PP1479	PROBEPOINT_SM	k2[7A6]
PP1480	PROBEPOINT_SM	k2[7A6]
PP1481	PROBEPOINT_SM	k2[7A6]
PP1482	PROBEPOINT_SM	k2[7A6]
PP1483	PROBEPOINT_SM	k2[7A6]
PP1484	PROBEPOINT_SM	k2[7A6]
PP1485	PROBEPOINT_SM	k2[7A6]
PP1486	PROBEPOINT_SM	k2[7A6]
PP1487	PROBEPOINT_SM	k2[7A6]
PP1488	PROBEPOINT_SM	k2[7A6]
PP1489	PROBEPOINT_SM	k2[7A6]
PP1490	PROBEPOINT_SM	k2[7A6]
PP1491	PROBEPOINT_SM	k2[7A6]
PP1492	PROBEPOINT_SM	k2[7A6]
PP1493	PROBEPOINT_SM	k2[7A6]
PP2100	PROBEPOINT_SM	k2[7C7]
PP2101	PROBEPOINT_SM	k2[7C7]
PP2102	PROBEPOINT_SM	k2[7C7]
PP2103	PROBEPOINT_SM	k2[7B7]
PP2104	PROBEPOINT_SM	k2[7B7]
PP2105	PROBEPOINT_SM	k2[7B7]
PP2106	PROBEPOINT_SM	k2[7B7]
PP2107	PROBEPOINT_SM	k2[7B7]
PP2108	PROBEPOINT_SM	k2[7B7]
PP2109	PROBEPOINT_SM	k2[7B7]
PP2110	PROBEPOINT_SM	k2[7B7]
PP2111	PROBEPOINT_SM	k2[7B7]
PP2112	PROBEPOINT_SM	k2[7B7]
PP2113	PROBEPOINT_SM	k2[7B7]
PP2114	PROBEPOINT_SM	k2[7B7]
PP2115	PROBEPOINT_SM	k2[7B7]
PP2116	PROBEPOINT_SM	k2[7B7]
PP2117	PROBEPOINT_SM	k2[7B7]
PP2118	PROBEPOINT_SM	k2[7B7]
PP2119	PROBEPOINT_SM	k2[7B7]
PP2120	PROBEPOINT_SM	k2[7B7]
PP2121	PROBEPOINT_SM	k2[7A7]
PP2122	PROBEPOINT_SM	k2[7A7]
PP2123	PROBEPOINT_SM	k2[7A7]
PP2124	PROBEPOINT_SM	k2[7A7]
PP2125	PROBEPOINT_SM	k2[7A7]
PP2126	PROBEPOINT_SM	k2[7A7]
PP2127	PROBEPOINT_SM	k2[7A7]
PP2128	PROBEPOINT_SM	k2[7A7]
PP2129	PROBEPOINT_SM	k2[7A7]
PP2130	PROBEPOINT_SM	k2[7A7]
PP2131	PROBEPOINT_SM	k2[7A7]
PP2132	PROBEPOINT_SM	k2[7B7]
PP2133	PROBEPOINT_SM	k2[7B7]
PP3700	PROBEPOINT_SM	k2[7D5]
PP3701	PROBEPOINT_SM	k2[7D5]
PP3702	PROBEPOINT_SM	k2[7D5]
PP3703	PROBEPOINT_SM	k2[7D5]
PP3704	PROBEPOINT_SM	k2[7D5]
PP4000	PROBEPOINT_SM	k2[7D5]
PP4001	PROBEPOINT_SM	k2[7D5]
PP4002	PROBEPOINT_SM	k2[7D5]
PP4003	PROBEPOINT_SM	k2[7D5]
PP4004	PROBEPOINT_SM	k2[7D5]
PP4900	PROBEPOINT_SM	k2[7C5]
PP4901	PROBEPOINT_SM	k2[7C5]
PP4902	PROBEPOINT_SM	k2[7C5]
PP4903	PROBEPOINT_SM	k2[7C5]
Q600	TRA_2N7002_SOT23-LF	k2[6A8]
Q610	TRA_2N7002_SOT23-LF	k2[6D7]
Q3800	TRA_PBSS5540Z_SOT223	k2[38C4]
Q3810	TRA_PBSS5540Z_SOT223	k2[38A4]
Q4200	TRA_BCP69_SOT223-4	k2[42D6]
Q4600	TRA_2N7002_SOT23-LF	k2[46C8]
Q5077	TRA_DUAL_MMDT3904_SO T-363-LF	k2[50D1 50D2]
Q5095	TRA_2N7002DW_SOT-363	k2[50C2 50C2]
Q5190	TRA_DUAL_MMDT3904_SO T-363-LF	k2[51B3 51C4]
Q5339	TRA_2N7002_SOT23-LF	k2[53B7]
Q5341	TRA_FDC796N_SUPERSOT -6	k2[53B6]
Q5570	TRA_2N7002DW_SOT-363	k2[55D1 55C2]
Q5600	TRA_NTHS5443T1_1206A -03-LF	k2[56D4]
Q5602	TRA_2N7002_SOT23-LF	k2[56D6]
Q5603	TRA_NTHS5443T1_1206A -03-LF	k2[56B4]
Q5605	TRA_2N7002_SOT23-LF	k2[56B6]
Q5700	TRA_NTHS5443T1_1206A -03-LF	k2[57D4]
Q5702	TRA_2N7002_SOT23-LF	k2[57C5]
Q7006	TRA_DUAL_SSM6N15FE_S OT563	k2[70A7 70B6]
Q7007	TRA_DUAL_SSM6N15FE_S OT563	k2[70A6 70B6]
Q7100	TRA_MOSFET_NCHN_5P1_ MLP5X6-LFPAK	k2[71D3]
Q7101	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[71D3]
Q7102	TRA_MOSFET_NCHN_5P1_ MLP5X6-LFPAK	k2[71C3]
Q7103	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[71B3]
Q7104	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[71C3]
Q7105	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[71B3]
Q7200	TRA_MOSFET_NCHN_5P1_ MLP5X6-LFPAK	k2[72C4]
Q7201	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[72C4]
Q7204	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[72C3]
Q7300	TRA_FDMS9620S_MLP	k2[73C6]
Q7360	TRA_FDMS9620S_MLP	k2[73C3]
Q7400	TRA_FDMS9620S_MLP	k2[74C6]
Q7460	TRA_FDM6296_MICROFET 3X3	k2[74C3]
Q7461	TRA_FDM6296_MICROFET 3X3	k2[74C3]
Q7520	TRA_MOSFET_NCHN_5P1_ MLP5X6-LFPAK	k2[75D4]
Q7521	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[75C4]
Q7603	TRA_2N7002_SOT23-LF	k2[76A6]
Q7620	TRA_FDMS9620S_MLP	k2[76C7]
Q7640	TRA_SINGLE_MOSFET_PC HN_SOT-23	k2[53B7]
Q7660	TRA_MOSFET_NCHN_5P1_ MLP5X6-LFPAK	k2[76C3]
Q7661	TRA_MOSFET_NCHN_5P2_ MLP5X6-LFPAK	k2[76B3]
Q7800	TRA_IRF7410_SO-8	k2[78D2]
Q7801	TRA_SINGLE_MOSFET_NC HN_SOT23	k2[78D3]
Q7810	TRA_IRF7410_SO-8	k2[78D6]
Q7811	TRA_SINGLE_MOSFET_NC HN_SOT23	k2[78D7]
Q7850	TRA_IRF7410_SO-8	k2[78C2]
Q7851	TRA_SINGLE_MOSFET_NC HN_SOT23	k2[78B3]
Q7895	TRA_MOSFET_NCHN_8P_S O-8	k2[78B6]
Q7896	TRA_2N7002_SOT23-LF	k2[78B7]
Q7897	TRA_SINGLE_MOSFET_NC HN_SOT23	k2[78B6]
Q9000	TRA_SI3443DV_TSOP-LF	k2[90C7]
Q9001	TRA_2N7002_SOT23-LF	k2[90B7]
Q9411	TRA_2N7002DW_SOT-363	k2[94D2 94C2]
R600	RES_402	k2[6A7]
R602	RES_402	k2[6A8]
R604	RES_402	k2[6B7]
R605	RES_603	k2[6A6]
R610	RES_402	k2[6D7]
R1002	RES_402	k2[10D5]
R1003	RES_402	k2[10C5]
R1004	RES_402	k2[10C5]
R1005	RES_402	k2[10B5]
R1006	RES_402	k2[10B5]
R1007	RES_402	k2[10A4]
R1012	RES_402	k2[10A4]
R1016	RES_402	k2[10B1]
R1017	RES_402	k2[10B1]
R1018	RES_402	k2[10B1]
R1019	RES_402	k2[10B1]
R1020	RES_402	k2[10B7]
R1021	RES_402	k2[10B7]
R1022	RES_402	k2[10A7]
R1023	RES_402	k2[10A7]
R1024	RES_402	k2[10A7]
R1030	RES_402	k2[10A4]
R1100	RES_402	k2[11B5]
R1101	RES_402	k2[11A5]
R1290	RES_402	k2[12C2]
R1291	RES_402	k2[12C2]
R1292	RES_402	k2[12C2]
R1293	RES_402	k2[12C2]
R1294	RES_402	k2[12C2]
R1295	RES_402	k2[12C2]
R1296	RES_402	k2[12C2]
R1303	RES_402	k2[13B2]
R1315	RES_402	k2[13C6]
R1330	RES_402	k2[13C5]
R1331	RES_402	k2[13C5]
R1399	RES_402	k2[13C7]
R1410	RES_402	k2[14B6]
R1411	RES_402	k2[14A6]
R1415	RES_402	k2[14A6]
R1420	RES_402	k2[14B6]
R1421	RES_402	k2[14B6]
R1425	RES_402	k2[14A7]
R1426	RES_402	k2[14A7]
R1510	RES_402	k2[15D3]
R1610	RES_402	k2[16C2]
R1611	RES_402	k2[16C2]
R1620	RES_402	k2[16C1]
R1622	RES_402	k2[16C1]
R1624	RES_402	k2[16C1]
R1630	RES_402	k2[16B7]
R1631	RES_402	k2[16B7]
R1640	RES_402	k2[16A3]
R1641	RES_402	k2[16A3]
R1655	RES_402	k2[16D7]
R1659	RES_402	k2[16D7]
R1666	RES_402	k2[16C7]
R1669	RES_402	k2[16C7]
R1670	RES_402	k2[16C7]
R1690	RES_402	k2[16A3]
R1691	RES_402	k2[16A3]
R2141	RES_603	k2[21B7]
R2145	RES_603	k2[21B7]
R2150	RES_603	k2[21A7]
R2170	RES_603	k2[21D4]
R2183	RES_402	k2[21C2]
R2185	RES_402	k2[21C3]
R2186	RES_402	k2[21B3]
R2190	RES_402	k2[21B3]
R2195	RES_402	k2[21A3]
R2200	RES_402	k2[22B2]
R2201	RES_402	k2[22A2]
R2202	RES_402	k2[22B2]
R2203	RES_402	k2[22A2]
R2300	RES_402	k2[23D7]
R2301	RES_402	k2[23D7]
R2302	RES_402	k2[23D6]
R2303	RES_402	k2[23D3]
R2304	RES_402	k2[23C3]
R2305	RES_402	k2[23C3]
R2306	RES_402	k2[23D3]
R2308	RES_402	k2[23C3]
R2309	RES_402	k2[23C3]
R2310	RES_402	k2[23D6]
R2311	RES_402	k2[23D6]
R2313	RES_402	k2[23C7]
R2314	RES_402	k2[23C7]
R2315	RES_402	k2[23C7]
R2316	RES_402	k2[23B7]
R2400	RES_402	k2[24C7]
R2401	RES_402	k2[24C7]
R2402	RES_402	k2[24C7]
R2403	RES_402	k2[24C7]
R2404	RES_402	k2[24C7]
R2405	RES_402	k2[24C6]
R2406	RES_402	k2[24B6]
R2407	RES_402	k2[24C6]
R2408	RES_402	k2[24C6]
R2409	RES_402	k2[24C6]
R2413	RES_402	k2[24C3]
R2414	RES_402	k2[24B3]
R2415	RES_402	k2[24B5]
R2423	RES_402	k2[24A3]
R2424	RES_402	k2[24A3]
R2425	RES_402	k2[24A3]
R2426	RES_402	k2[24A3]
R2427	RES_402	k2[24A3]
R2428	RES_402	k2[24A3]
R2429	RES_402	k2[24A3]
R2430	RES_402	k2[24A3]
R2431	RES_402	k2[24A3]
R2432	RES_402	k2[24A3]
R2433	RES_402	k2[24A3]
R2436	RES_402	k2[24A3]
R2437	RES_402	k2[24A3]
R2438	RES_402	k2[24A3]
R2439	RES_402	k2[24A3]
R2440	RES_402	k2[24A3]
R2441	RES_402	k2[24A3]
R2442	RES_402	k2[24A3]
R2500	RES_402	k2[25D7]
R2502	RES_402	k2[25D7]
R2504	RES_402	k2[25D6]
R2505	RES_402	k2[25D6]
R2506	RES_402	k2[25D6]
R2507	RES_402	k2[25D6]
R2510	RES_402	k2[25D6]
R2511	RES_402	k2[25A8]
R2512	RES_402	k2[25A8]
R2514	RES_402	k2[25A7]
R2515	RES_402	k2[25A7]
R2516	RES_402	k2[25A7]
R2523	RES_402	k2[25B3]
R2524	RES_402	k2[25C2]
R2525	RES_402	k2[25C2]
R2526	RES_402	k2[25C2]
R2527	RES_402	k2[25B2]
R2528	RES_402	k2[25B2]
R2529	RES_402	k2[25B2]
R2530	RES_402	k2[25B4]
R2531	RES_402	k2[25B4]
R2532	RES_402	k2[25D3]
R2533	RES_402	k2[25D2]
R2534	RES_402	k2[25D2]
R2535	RES_402	k2[25D3]
R2536	RES_402	k2[25A4]
R2544	RES_402	k2[25A4]
R2545	RES_402	k2[25A4]
R2546	RES_402	k2[25A4]
R2547	RES_402	k2[25D6]
R2550	RES_402	k2[25D7]
R2551	RES_402	k2[25D7]
R2552	RES_402	k2[25D7]
R2553	RES_402	k2[25D7]
R2596	RES_402	k2[25A4]
R2597	RES_402	k2[25A4]
R2598	RES_402	k2[25A4]
R2700	RES_603	k2[27A8]
R2701	RES_402	k2[27D8]
R2702	RES_402	k2[27D8]
R2710	RES_402	k2[28B2]
R2735	RES_402	k2[27A8]
R2800	RES_402	k2[28D5]
R2803	RES_402	k2[28A6]
R2806	RES_402	k2[28D6]
R2807	RES_402	k2[28D7]
R2809	RES_402	k2[28C7]
R2810	RES_402	k2[28C7]
R2850	RES_402	k2[28B1]
R2881	RES_402	k2[28D2]
R2883	RES_402	k2[28D2]
R2885	RES_402	k2[28D2]
R2890	RES_402	k2[28C2]
R2891	RES_402	k2[28D2]
R2892	RES_402	k2[28C2]
R2893	RES_402	k2[28C2]
R2896	RES_402	k2[28A4]
R2897	RES_402	k2[28A4]
R2900	RES_402	k2[29C6]
R2901	RES_402	k2[29D3]
R2902	RES_402	k2[29C3]
R2903	RES_402	k2[29B6]
R3026	RES_402	k2[30A4]
R3027	RES_402	k2[30A4]
R3030	RES_402	k2[30A4]
R3032	RES_402	k2[30C7]
R3033	RES_402	k2[30C7]
R3034	RES_402	k2[30A7]
R3035	RES_402	k2[30A7]
R3046	RES_402	k2[30C1]
R3047	RES_402	k2[30C1]
R3050	RES_402	k2[30D1]
R3051	RES_402	k2[30D1]
R3052	RES_402	k2[30D1]
R3053	RES_402	k2[30C1]
R3054	RES_402	k2[30C1]
R3055	RES_402	k2[30C1]
R3067	RES_402	k2[30D7]
R3080	RES_402	k2[30C7]
R3081	RES_402	k2[30C7]
R3082	RES_402	k2[30C7]
R3083	RES_402	k2[30C7]
R3084	RES_402	k2[30B7]
R3085	RES_402	k2[30B7]
R3086	RES_402	k2[30B7]
R3087	RES_402	k2[30B7]
R3088	RES_402	k2[30B7]
R3089	RES_402	k2[30B7]
R3090	RES_402	k2[30B7]
R3091	RES_402	k2[30B7]
R3098	RES_402	k2[30B4]
R3100	RES_402	k2[31D2]
R3101	RES_402	k2[31C2]
R3140	RES_402	k2[31A3]
R3141	RES_402	k2[31A3]
R3200	RES_402	k2[32C2]
R3201	RES_402	k2[32C2]
R3240	RES_402	k2[32A3]
R3241	RES_402	k2[32A3]
R3300	RES_402	k2[33D5]
R3301	RES_402	k2[33D5]
R3302	RES_402	k2[33D5]
R3303	RES_402	k2[33D5]
R3304	RES_402	k2[33C5]
R3305	RES_402	k2[33C5]
R3400	RES_402	k2[34C7]
R3401	RES_402	k2[34C7]
R3410	RES_402	k2[34A5]
R3720	RES_402	k2[37C6]
R3740	RES_402	k2[37B7]
R3741	RES_402	k2[37B7]
R3742	RES_402	k2[37B6]
R3743	RES_402	k2[37B6]
R3744	RES_402	k2[37B6]
R3745	RES_402	k2[37B5]
R3746	RES_402	k2[37B5]
R3747	RES_402	k2[37B5]
R3760	RES_402	k2[37C2]
R3765	RES_402	k2[37B2]
R3780	RES_402	k2[37B2]
R3781	RES_402	k2[37B2]
R3801	RES_402	k2[38C4]
R3811	RES_402	k2[38A5]
R3900	RES_402	k2[39D7]
R3901	RES_603	k2[39A7]
R3902	RES_603	k2[39A7]
R3903	RES_603	k2[39A7]
R3904	RES_603	k2[39A6]
R3910	RES_402	k2[39A4]
R3911	RES_402	k2[39A4]
R3912	RES_402	k2[39A4]
R3913	RES_402	k2[39A4]
R4000	RES_402	k2[40B6]
R4001	RES_402	k2[40C7]
R4002	RES_402	k2[40C7]
R4010	RES_402	k2[40C2]
R4011	RES_402	k2[40B2]
R4012	RES_402	k2[40B2]
R4013	RES_402	k2[40C2]
R4080	RES_402	k2[40B8]
R4090	RES_402	k2[40B6]
R4200	RES_402	k2[42C7]
R4250	RES_402	k2[42D3]
R4251	RES_402	k2[42D2]
R4252	RES_402	k2[42D2]
R4260	RES_402	k2[42C3]
R4261	RES_402	k2[42C2]
R4262	RES_402	k2[42C2]
R4300	RES_2512	k2[43D7]
R4301	RES_2512	k2[43D7]
R4302	RES_805	k2[43D7]
R4335	RES_402	k2[43B2]
R4350	RES_402	k2[43C7]
R4351	RES_402	k2[43C7]
R4352	RES_402	k2[43B7]
R4353	RES_402	k2[43B7]
R4354	RES_402	k2[43B7]
R4360	RES_402	k2[43C7]
R4361	RES_402	k2[43C7]
R4362	RES_402	k2[43B7]
R4363	RES_402	k2[43B7]
R4364	RES_402	k2[43B7]
R4390	RES_402	k2[43A7]
R4403	RES_402	k2[44C5]
R4451	RES_402	k2[44C5]
R4453	RES_402	k2[44C4]
R4454	RES_402	k2[44C4]
R4457	RES_402	k2[44B6]
R4458	RES_402	k2[44B5]
R4459	RES_402	k2[44B5]
R4590	RES_402	k2[45B1]
R4599	RES_603	k2[45C2]
R4600	RES_402	k2[46D8]
R4650	RES_402	k2[46D4]
R4651	RES_402	k2[46C4]
R4652	RES_402	k2[46C4]
R4701	RES_402	k2[47B6]
R4702	RES_402	k2[47B6]
R4710	RES_402	k2[47A6]
R4711	RES_402	k2[47A6]
R4721	RES_402	k2[47D1]
R4901	RES_402	k2[49C1]
R4902	RES_402	k2[49C2]
R4903	RES_402	k2[49C1]
R4909	RES_402	k2[49C1]
R4950	RES_402	k2[49C4]
R4951	RES_402	k2[49C4]
R4998	RES_402	k2[49C2]
R4999	RES_402	k2[49D4]
R5000	RES_402	k2[50D6]
R5010	RES_402	k2[50C6]
R5032	RES_402	k2[50B1]
R5033	RES_402	k2[50B1]
R5034	RES_402	k2[50B1]
R5035	RES_402	k2[50B1]
R5036	RES_402	k2[50B1]
R5037	RES_402	k2[50B1]
R5038	RES_402	k2[50B1]
R5039	RES_402	k2[50B1]
R5040	RES_402	k2[50B1]

R5041	RES_402	k2[50B1]
R5042	RES_402	k2[50B1]
R5043	RES_402	k2[50B1]
R5046	RES_402	k2[50A1]
R5047	RES_402	k2[50B1]
R5048	RES_402	k2[50A1]
R5070	RES_402	k2[50D2]
R5071	RES_402	k2[50D3]
R5078	RES_402	k2[50D1]
R5080	RES_402	k2[50B1]
R5082	RES_402	k2[50B1]
R5083	RES_402	k2[50A1]
R5084	RES_402	k2[50A1]
R5088	RES_402	k2[50A1]
R5090	RES_402	k2[50B1]
R5091	RES_402	k2[50B1]
R5092	RES_402	k2[50B1]
R5093	RES_402	k2[50B1]
R5094	RES_402	k2[50B1]
R5096	RES_402	k2[50B1]
R5190	RES_402	k2[51B2]
R5191	RES_402	k2[51C3]
R5192	RES_402	k2[51C4]
R5200	RES_402	k2[52D7]
R5201	RES_402	k2[52D7]
R5230	RES_402	k2[52A7]
R5231	RES_402	k2[52A7]
R5250	RES_402	k2[52D4]
R5251	RES_402	k2[52D4]
R5260	RES_402	k2[52C4]
R5261	RES_402	k2[52C4]
R5270	RES_402	k2[52D2]
R5271	RES_402	k2[52D2]
R5280	RES_402	k2[52C2]
R5281	RES_402	k2[52C2]
R5290	RES_402	k2[52B2]
R5291	RES_402	k2[52B2]
R5309	RES_402	k2[53D7]
R5339	RES_402	k2[53B7]
R5340	RES_402	k2[53A8]
R5341	RES_402	k2[53B7]
R5342	RES_402	k2[53B7]
R5343	RES_1206	k2[53B5]
R5353	RES_402	k2[53D4]
R5354	RES_402	k2[53D4]
R5370	RES_402	k2[53C7]
R5380	RES_SENSE_2512-1	k2[53D3]
R5381	RES_SENSE_2512-1	k2[53C4]
R5382	RES_SENSE_2512	k2[53B4]
R5383	RES_402	k2[53B2]
R5384	RES_402	k2[53B2]
R5385	RES_402	k2[53B4]
R5386	RES_402	k2[53A4]
R5387	RES_402	k2[53B3]
R5388	RES_402	k2[53A3]
R5500	RES_402	k2[55B2]
R5501	RES_402	k2[55A2]
R5510	RES_402	k2[55B3]
R5511	RES_402	k2[55B3]
R5512	RES_402	k2[55B3]
R5570	RES_402	k2[55D4]
R5571	RES_402	k2[55D2]
R5572	RES_402	k2[55D2]
R5573	RES_402	k2[55D2]
R5600	RES_402	k2[56C7]
R5601	RES_402	k2[56A7]
R5602	RES_1206	k2[56D6]
R5603	RES_805	k2[56D5]
R5605	RES_805	k2[56D5]
R5606	RES_402	k2[56D6]
R5607	RES_805	k2[56B5]
R5609	RES_805	k2[56B5]
R5610	RES_1206	k2[56B6]
R5611	RES_402	k2[56B6]
R5698	RES_402	k2[56A7]
R5699	RES_402	k2[56C7]
R5700	RES_402	k2[57C7]
R5701	RES_805	k2[57D5]
R5703	RES_805	k2[57D5]
R5704	RES_1206	k2[57D5]
R5705	RES_402	k2[57D6]
R5797	RES_402	k2[57C8]
R6100	RES_402	k2[61C5]
R6101	RES_402	k2[61C5]
R6114	RES_402	k2[61B4]
R6190	RES_402	k2[61B6]
R6191	RES_402	k2[61B6]
R6193	RES_402	k2[61B3]
R7000	RES_402	k2[70D8]
R7001	RES_402	k2[70D8]
R7002	RES_402	k2[70C8]
R7003	RES_402	k2[70C8]
R7005	RES_402	k2[70D5]
R7006	RES_402	k2[70D5]
R7007	RES_402	k2[70D5]
R7008	RES_402	k2[70D5]
R7010	RES_402	k2[70D7]
R7011	RES_402	k2[70C7]
R7013	RES_402	k2[70D7]
R7014	RES_402	k2[70C7]
R7018	RES_402	k2[70D7]
R7019	RES_402	k2[70C7]
R7020	RES_402	k2[70D7]
R7021	RES_402	k2[70C7]
R7030	RES_402	k2[70C3]
R7031	RES_402	k2[70C3]
R7032	RES_402	k2[70C3]
R7034	RES_402	k2[70D3]
R7035	RES_402	k2[70B3]
R7036	RES_402	k2[70B3]
R7037	RES_402	k2[70B3]
R7038	RES_402	k2[70B3]
R7039	RES_402	k2[70C3]
R7040	RES_402	k2[70C7]
R7041	RES_402	k2[70B7]
R7060	RES_402	k2[70A7]
R7061	RES_402	k2[70A6]
R7062	RES_402	k2[70A6]
R7063	RES_402	k2[70B6]
R7064	RES_402	k2[70B6]
R7065	RES_402	k2[70C6]
R7066	RES_402	k2[70C6]
R7070	RES_402	k2[70C7]
R7080	RES_402	k2[70D3]
R7081	RES_402	k2[70D3]
R7092	RES_402	k2[70B3]
R7100	RES_402	k2[71C2]
R7101	RES_603	k2[71C2]
R7102	RES_1206	k2[71B3]
R7103	RES_1206	k2[71D3]
R7104	RES_402	k2[71C1]
R7105	RES_402	k2[71B2]
R7106	RES_603	k2[71B2]
R7107	RES_402	k2[71B1]
R7108	RES_402	k2[71C8]
R7109	RES_402	k2[71B7]
R7110	RES_402	k2[71B7]
R7111	RES_402	k2[71B8]
R7112	RES_402	k2[71D7]
R7114	RES_402	k2[71B7]
R7115	RES_402	k2[71B4]
R7116	RES_402	k2[71B4]
R7117	RES_402	k2[71B5]
R7118	RES_402	k2[71B5]
R7119	RES_402	k2[71C8]
R7120	RES_402	k2[71D7]
R7121	RES_402	k2[71D7]
R7122	RES_402	k2[71A4]
R7123	RES_402	k2[71A4]
R7126	THERMISTER_402	k2[71C8]
R7127	RES_402	k2[71C7]
R7130	RES_402	k2[71B4]
R7131	THERMISTER_0603-LF	k2[71B4]
R7140	RES_603	k2[71B1]
R7141	RES_603	k2[71C1]
R7142	RES_402	k2[71D4]
R7143	RES_402	k2[71C4]
R7197	RES_402	k2[71D6]
R7199	RES_402	k2[71C7]
R7200	RES_402	k2[72C3]
R7201	RES_603	k2[72B3]
R7203	RES_1206	k2[72C3]
R7204	RES_402	k2[72C2]
R7241	RES_603	k2[72C2]
R7250	RES_402	k2[72C5]
R7300	RES_402	k2[73B7]
R7301	RES_402	k2[73B7]
R7306	RES_1206	k2[73C7]
R7310	RES_1206	k2[73A3]
R7311	RES_1206	k2[73A3]
R7312	RES_1206	k2[73A3]
R7313	RES_1206	k2[73A3]
R7321	RES_402	k2[73C5]
R7323	RES_402	k2[73B5]
R7331	RES_402	k2[73C5]
R7356	RES_1206	k2[73C2]
R7361	RES_402	k2[73C3]
R7371	RES_402	k2[73C3]
R7382	RES_402	k2[73C4]
R7383	RES_402	k2[73B4]
R7384	RES_402	k2[73B4]
R7390	RES_402	k2[73B2]
R7391	RES_402	k2[73B2]
R7400	RES_402	k2[74B7]
R7401	RES_402	k2[74B7]
R7406	RES_1206	k2[74C7]
R7421	RES_402	k2[74C5]
R7423	RES_402	k2[74B5]
R7431	RES_402	k2[74C5]
R7456	RES_1206	k2[74C2]
R7461	RES_402	k2[74C4]
R7471	RES_402	k2[74C3]
R7483	RES_402	k2[74B4]
R7490	RES_402	k2[74B2]
R7491	RES_402	k2[74B2]
R7500	RES_402	k2[75D5]
R7501	RES_402	k2[75C2]
R7504	RES_402	k2[75D7]
R7505	RES_402	k2[75C7]
R7506	RES_402	k2[75C7]
R7507	RES_402	k2[75D5]
R7508	RES_402	k2[75C7]
R7510	RES_402	k2[75C4]
R7521	RES_402	k2[75C1]
R7522	RES_402	k2[75C1]
R7539	RES_402	k2[75D6]
R7551	RES_402	k2[75B5]
R7556	RES_1206	k2[75C3]
R7600	RES_402	k2[76C5]
R7601	RES_402	k2[76A7]
R7602	RES_402	k2[76A7]
R7603	RES_402	k2[76A3]
R7604	RES_402	k2[76A3]
R7606	RES_402	k2[76A4]
R7607	RES_402	k2[76A4]
R7612	RES_402	k2[76A6]
R7613	RES_402	k2[76D7]
R7614	RES_402	k2[76D7]
R7615	RES_402	k2[76D7]
R7616	RES_402	k2[76D7]
R7617	RES_402	k2[76D7]
R7618	RES_402	k2[76D6]
R7621	RES_402	k2[76C7]
R7624	RES_402	k2[76C6]
R7625	RES_402	k2[76B6]
R7626	RES_402	k2[76C7]
R7627	RES_402	k2[76B7]
R7628	RES_402	k2[76B7]
R7629	RES_402	k2[76C7]
R7630	RES_402	k2[76A7]
R7631	RES_402	k2[76A7]
R7661	RES_402	k2[76C2]
R7664	RES_402	k2[76C3]
R7665	RES_402	k2[76B4]
R7666	RES_402	k2[76C2]
R7667	RES_402	k2[76B2]
R7668	RES_402	k2[76B2]
R7669	RES_402	k2[76C2]
R7670	RES_402	k2[76C4]
R7692	RES_402	k2[76A6]
R7710	RES_402	k2[77D6]
R7711	RES_402	k2[77D6]
R7712	RES_402	k2[77D4]
R7713	RES_402	k2[77C4]
R7800	RES_402	k2[78D3]
R7801	RES_402	k2[78D3]
R7810	RES_402	k2[78D7]
R7811	RES_402	k2[78D6]
R7850	RES_402	k2[78B3]
R7851	RES_402	k2[78B3]
R7870	RES_402	k2[78C7]
R7895	RES_402	k2[78B7]
R7896	RES_402	k2[78B6]
R7897	RES_402	k2[78B6]
R7898	RES_402	k2[78B6]
R8500	RES_402	k2[85C7]
R8501	RES_402	k2[85C5]
R8502	RES_402	k2[85C7]
R8503	RES_402	k2[85A4]
R8505	RES_402	k2[85B4]
R8570	RES_402	k2[85D3]
R9000	RES_402	k2[90C8]
R9001	RES_402	k2[90C7]
R9002	RES_805	k2[90C8]
R9003	RES_805	k2[90C8]
R9070	RES_402	k2[90B7]
R9074	RES_402	k2[90B2]
R9075	RES_402	k2[90B2]
R9090	RES_805	k2[90C6]
R9099	RES_402	k2[90C8]
R9140	RES_402	k2[91A6]
R9141	RES_402	k2[91B6]
R9142	RES_402	k2[91B6]
R9160	RES_402	k2[91B3]
R9161	RES_402	k2[91A3]
R9400	RES_402	k2[94D7]
R9402	RES_402	k2[94D7]
R9403	RES_402	k2[94D7]
R9404	RES_402	k2[94C7]
R9405	RES_402	k2[94C7]
R9408	RES_402	k2[94C7]
R9409	RES_402	k2[94C7]
R9410	RES_402	k2[94D2]
R9411	RES_402	k2[94D2]
R9412	RES_402	k2[94D2]
R9413	RES_402	k2[94C2]
R9414	RES_402	k2[94C2]
R9415	RES_402	k2[94B7]
R9420	RES_402	k2[94D1]
R9421	RES_402	k2[94D1]
R9422	RES_402	k2[94C2]
R9800	RES_402	k2[98C6]
R9801	RES_402	k2[98B6]
RP3300	RPAK4P_SM-LF	k2[33C4 33C4 33C4 33C4]
RP3305	RPAK4P_SM-LF	k2[33B4 33C4 33C4 33C4]
RP3310	RPAK4P_SM-LF	k2[33D4 33A4 33A4 33A4]
RP3330	RPAK4P_SM-LF	k2[33D4 33B4 33B4 33B4]
RP3334	RPAK4P_SM-LF	k2[33B4 33B4 33B4 33B4]
RP3338	RPAK4P_SM-LF	k2[33A4 33B4 33B4 33A4]
RP3342	RPAK4P_SM-LF	k2[33B4 33C4 33C4 33C4]
RP3346	RPAK4P_SM-LF	k2[33D4 33C4 33B4 33C4]
RP3350	RPAK4P_SM-LF	k2[33B4 33A4 33B4 33B4]
RP3354	RPAK4P_SM-LF	k2[33B4 33A4 33A4 33B4]
RP3358	RPAK4P_SM-LF	k2[33C4 33C4 33C4 33C4]
RP3362	RPAK4P_SM-LF	k2[33A4 33C4 33D4 33A4]
S5000	SWI_TACT_4SM_EVQPH_S M-LF	k2[50D8]
S5010	SWI_TACT_4SM_EVQPH_S M-LF	k2[50C7]
SC0700	SPRING_CLIP_1P_EMI_C LIP-SM1	k2[7B6]
SC0701	SPRING_CLIP_1P_EMI_C LIP-SM1	k2[7B5]
SC0702	SPRING_CLIP_1P_EMI_C LIP-SM-K2	k2[7B5]
SDF0717	PCB_STANDOFF	k2[7A3]
SDF0721	PCB_STANDOFF	k2[7A2]
SDF0724	PCB_STANDOFF	k2[7A6]
SDF0726	HSK_NUT_TH	k2[7A5]
SDF0727	HSK_NUT_TH	k2[7A5]
SDF3400	PCB_STANDOFF	k2[34A5]
SDF4721	PCB_STANDOFF	k2[47D1]
SDF9000	PCB_STANDOFF	k2[90B7]
SDF9001	PCB_STANDOFF	k2[90A7]
SDF9800	PCB_STANDOFF	k2[98D5]
SDF9801	PCB_STANDOFF	k2[98D5]
SDF9803	PCB_STANDOFF	k2[98B5]
SDF9804	PCB_STANDOFF	k2[98B5]
SW2800	SWI_TACT_4SM_EVQPH_S M-LF	k2[28A4]
T3900	XFR_LFE9245A_SOI	k2[39C5]
U1400	CRESTLINE_FCBGA	k2[14D4]
U1400	CRESTLINE_FCBGA	k2[15D4]
U1400	CRESTLINE_FCBGA	k2[16D5]
U1400	CRESTLINE_FCBGA	k2[17D3 17D7]
U1400	CRESTLINE_FCBGA	k2[18D3 18D7]
U1400	CRESTLINE_FCBGA	k2[19D5]
U1400	CRESTLINE_FCBGA	k2[20D4 20D7]
U2300	SB_ICH8M_BGA	k2[23D5]
U2300	SB_ICH8M_BGA	k2[24B7 24D4]
U2300	SB_ICH8M_BGA	k2[25D4]
U2300	SB_ICH8M_BGA	k2[26D5 26D8]
U2803	MC74VHC1G00_SC70-5	k2[28A7]
U2900	CLK_SYN_SLG8LP537_QF N	k2[29C5]
U3700	88E8058_QFN	k2[37C4]
U3780	EEPROM_M24C08_SO8	k2[37B2]
U4000	FW643_BGA	k2[40C5]
U4600	SWI_TPS2068_MSOP	k2[46C7]
U4601	SWI_TPS2068_MSOP	k2[46D7]
U4650	PI3USB10_TDFN	k2[46D4]
U4900	SMC_H8S2116_BGA	k2[49A3 49C3 49B7 49D7]
U5000	VDET_RN5VD_SOT23-5A	k2[50D7]
U5380	MAX4073_SC70	k2[53C4]
U5381	MAX4377_UMAX	k2[53B3]
U5500	LM95214_LLP	k2[55B4]
U5570	EMC1402_MSOP	k2[55D4]
U6100	FLASH_SST25VF016B_SO I_SOI	k2[61C5]
U7010	COMPARATOR_LM339A_SO I-LF	k2[70D6]
U7052	MC74VHC1G08_SOT23-5- LF	k2[70C2]
U7056	MC74VHC1G08_SOT23-5- LF	k2[70C2]
U7100	ISL6260C_QFN	k2[71C6]
U7101	ISL6208_QFN	k2[71D5]
U7102	ISL6208_QFN	k2[71C5]
U7201	ISL6208_QFN	k2[72C7]
U7300	ISL6539_SSOP	k2[73C5]
U7400	ISL6539_SSOP	k2[74C5]
U7500	ISL6269_QFN	k2[75D6]
U7501	SN74LVC1G07_SC70	k2[75D8]
U7550	LREG_BD3533FVM_MSOP-8	k2[75B4]
U7600	LTC3728L_QFN	k2[76C5]
U7601	COMPARATOR_LM393_SOI -1-LF	k2[76D6 76A7]
U7710	TPS62050_MSOP	k2[77D5]
U7750	VREG_TA48025BF_HSOP3	k2[77B5]
U8570	EEPROM_M24C02_SO8	k2[85D2]
U9130	VIDEO_TS3V330_SOP	k2[91B7]
U9160	74LVC1G125LF_SOT23-5	k2[91B4]
U9161	74LVC1G125LF_SOT23-5	k2[91A4]
VR5065	VREF_REF3133_SOT23-3	k2[50B8]
XW4900	SHORT_SM	k2[49C2]
XW5309	SHORT_SM	k2[53D7]
XW5500	SHORT_SM	k2[55A4]
XW5501	SHORT_SM	k2[55A4]
XW5502	SHORT_SM	k2[55A4]
XW5503	SHORT_SM	k2[55A4]
XW7100	SHORT_SM	k2[71A6]
XW7101	SHORT_SM	k2[71B2]
XW7102	SHORT_SM	k2[71B1]
XW7103	SHORT_SM	k2[71D2]
XW7104	SHORT_SM	k2[71D1]
XW7203	SHORT_SM	k2[72C3]
XW7204	SHORT_SM	k2[72C2]
XW7300	SHORT_SM	k2[73B4]
XW7400	SHORT_SM	k2[74B4]
XW7500	SHORT_SM	k2[75C5]
XW7600	SHORT_SM	k2[76A5]
Y2800	CRYSTAL_4PIN_SM-LF	k2[28C7]
Y2901	CRYSTAL_5X3.2-SM	k2[29C6]
Y3750	CRYSTAL_SM-3-LF	k2[37B5]
Y4000	CRYSTAL_HC49-USMD	k2[40B7]
Y5020	CRYSTAL_SM-4	k2[50C8]
ZH500	HOLE_VIA	k2[7C1]
ZH501	HOLE_VIA	k2[7C1]
ZH502	HOLE_VIA	k2[7C1]
ZH503	HOLE_VIA	k2[7C1]
ZH504	HOLE_VIA	k2[7B1]
ZH505	HOLE_VIA	k2[7B1]
ZH506	HOLE_VIA	k2[7B1]
ZH507	HOLE_VIA	k2[7B1]
ZH508	HOLE_VIA	k2[7B1]
ZH509	HOLE_VIA	k2[7B1]
ZH510	HOLE_VIA	k2[7C1]
ZH511	HOLE_VIA	k2[7C1]
ZH512	HOLE_VIA	k2[7C1]
ZH513	HOLE_VIA	k2[7C1]
ZH514	HOLE_VIA	k2[7B1]
ZH515	HOLE_VIA	k2[7B1]
ZH516	HOLE_VIA	k2[7B1]
ZH517	HOLE_VIA	k2[7B1]
ZH518	HOLE_VIA	k2[7B1]
ZH519	HOLE_VIA	k2[7B1]
ZH520	HOLE_VIA	k2[7C1]
ZH521	HOLE_VIA	k2[7C1]
ZH522	HOLE_VIA	k2[7C1]
ZH523	HOLE_VIA	k2[7C1]
ZH524	HOLE_VIA	k2[7B1]
ZH525	HOLE_VIA	k2[7B1]
ZH526	HOLE_VIA	k2[7B1]
ZH527	HOLE_VIA	k2[7B1]
ZH528	HOLE_VIA	k2[7B1]
ZH529	HOLE_VIA	k2[7B1]
ZH0700	MTGHOLE	k2[7A3]
ZH0701	MTGHOLE	k2[7A3]
ZH0702	MTGHOLE	k2[7A3]
ZH0703	MTGHOLE	k2[7A2]
ZH0710	MTGHOLE	k2[7A6]
ZH0711	MTGHOLE	k2[7A5]
ZH0712	MTGHOLE	k2[7A5]
ZH0713	MTGHOLE	k2[7A5]
ZH0714	MTGHOLE	k2[7A4]
ZH0715	MTGHOLE	k2[7A4]
ZH0718	MTGHOLE	k2[7A3]
ZH0719	MTGHOLE	k2[7A3]
ZH0720	MTGHOLE	k2[7A3]
ZH0722	MTGHOLE	k2[7A4]
ZH0723	MTGHOLE	k2[7A4]
ZH0725	MTGHOLE	k2[7A4]